Microsystems Technology Office Brief to GAN Industry Day

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Dr. John C. Zolper, Deputy Director

2 August 2004

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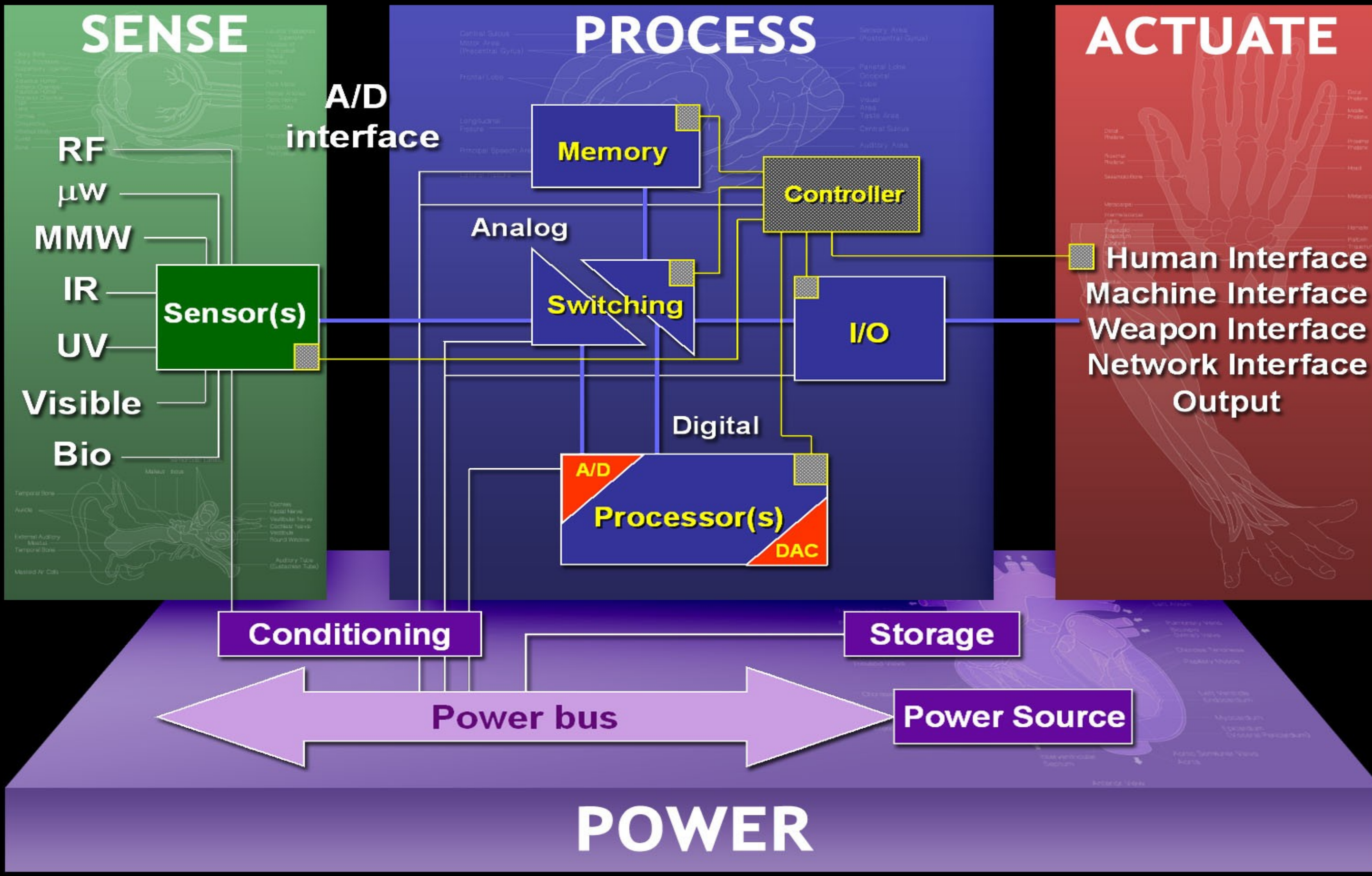
Integrated Microsystem



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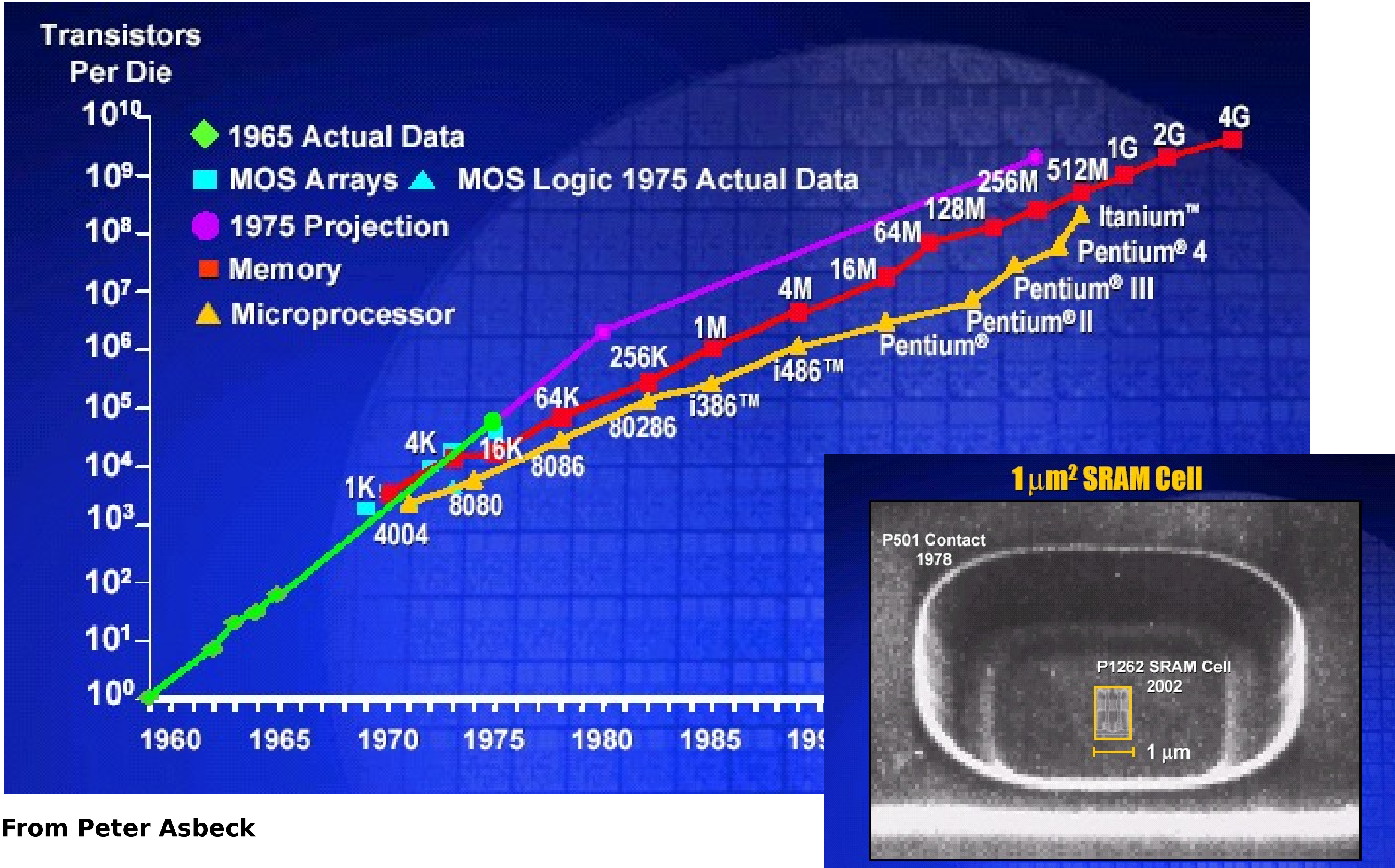
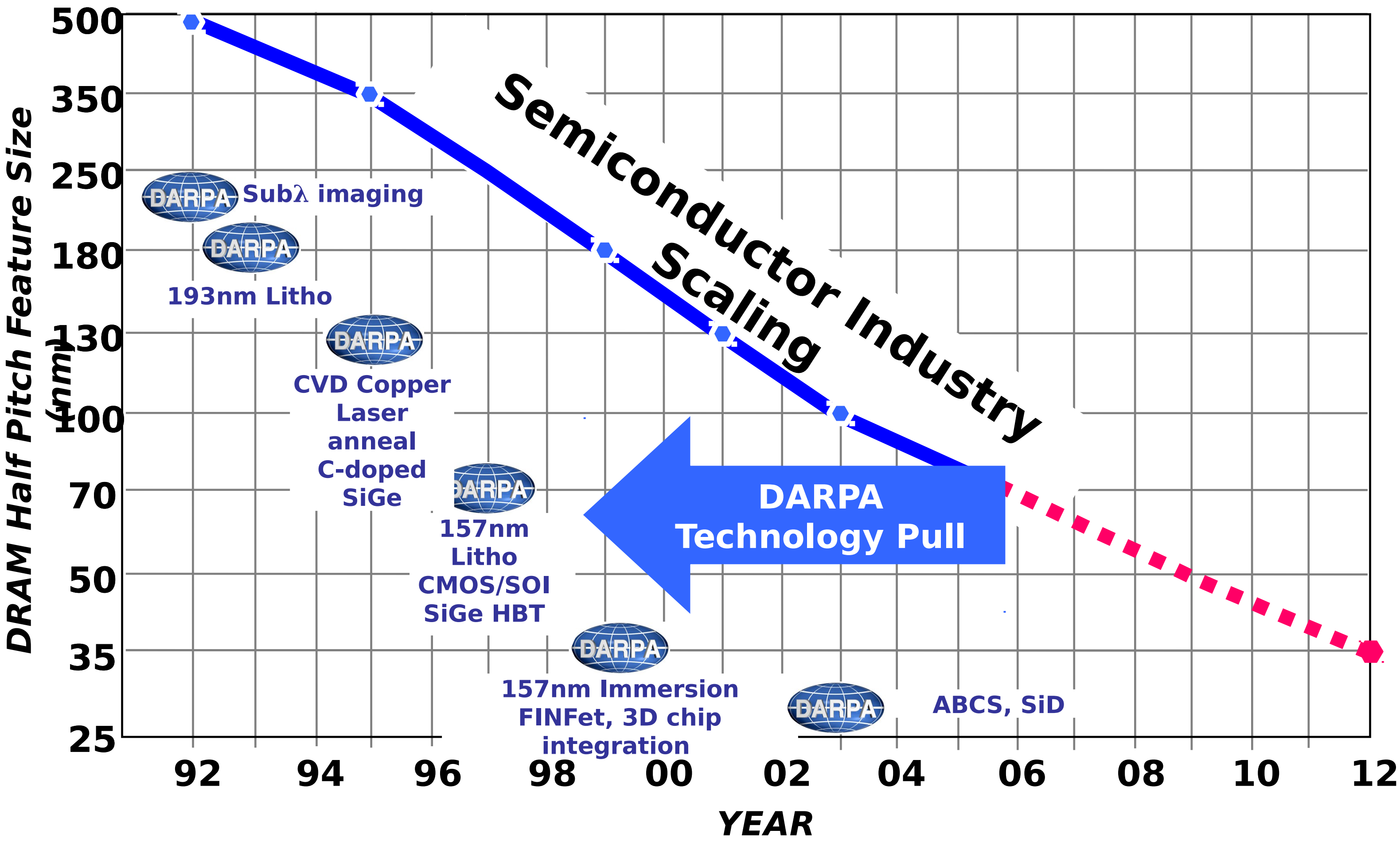
Moore's Law Scaling

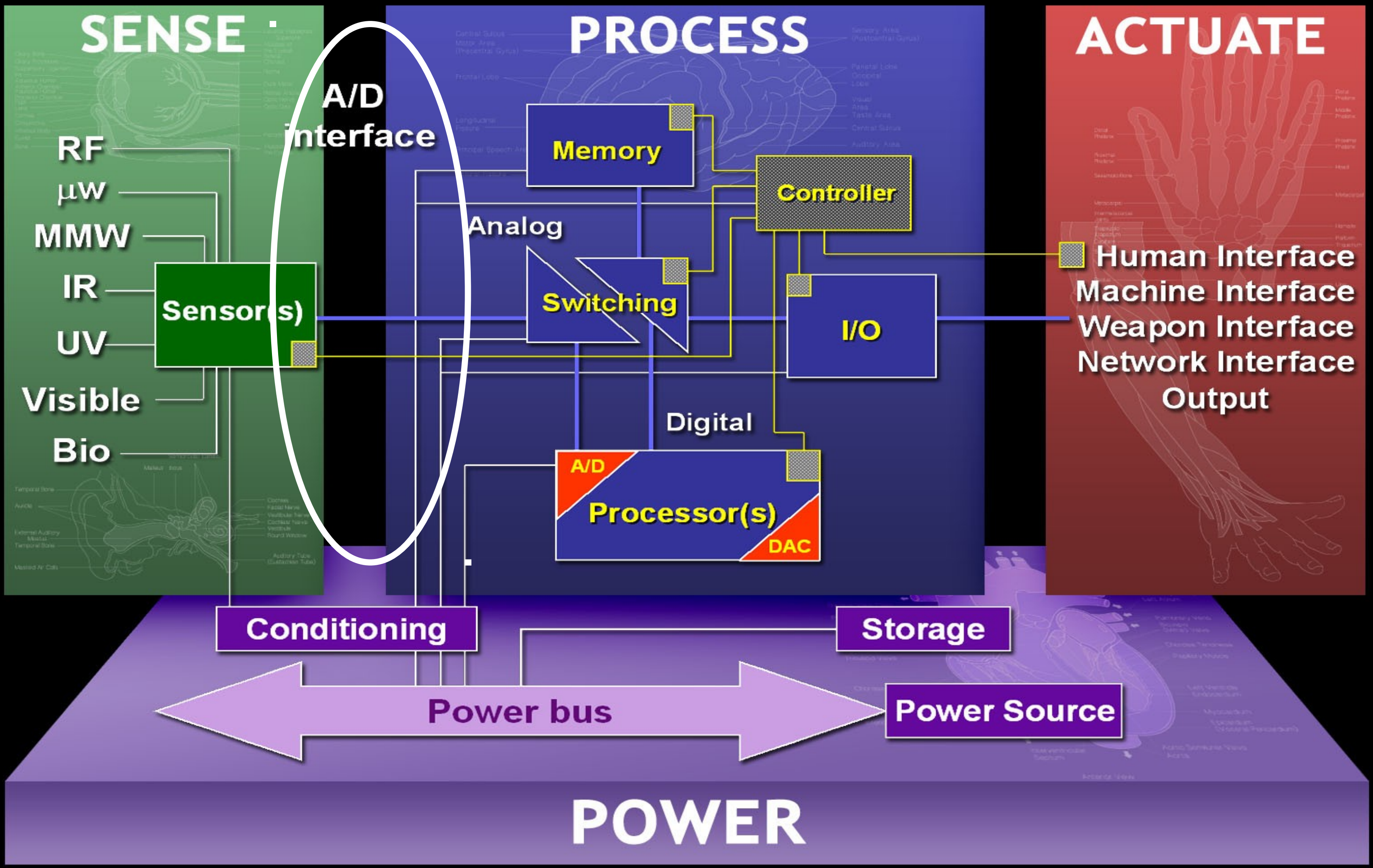


From Peter Asbeck

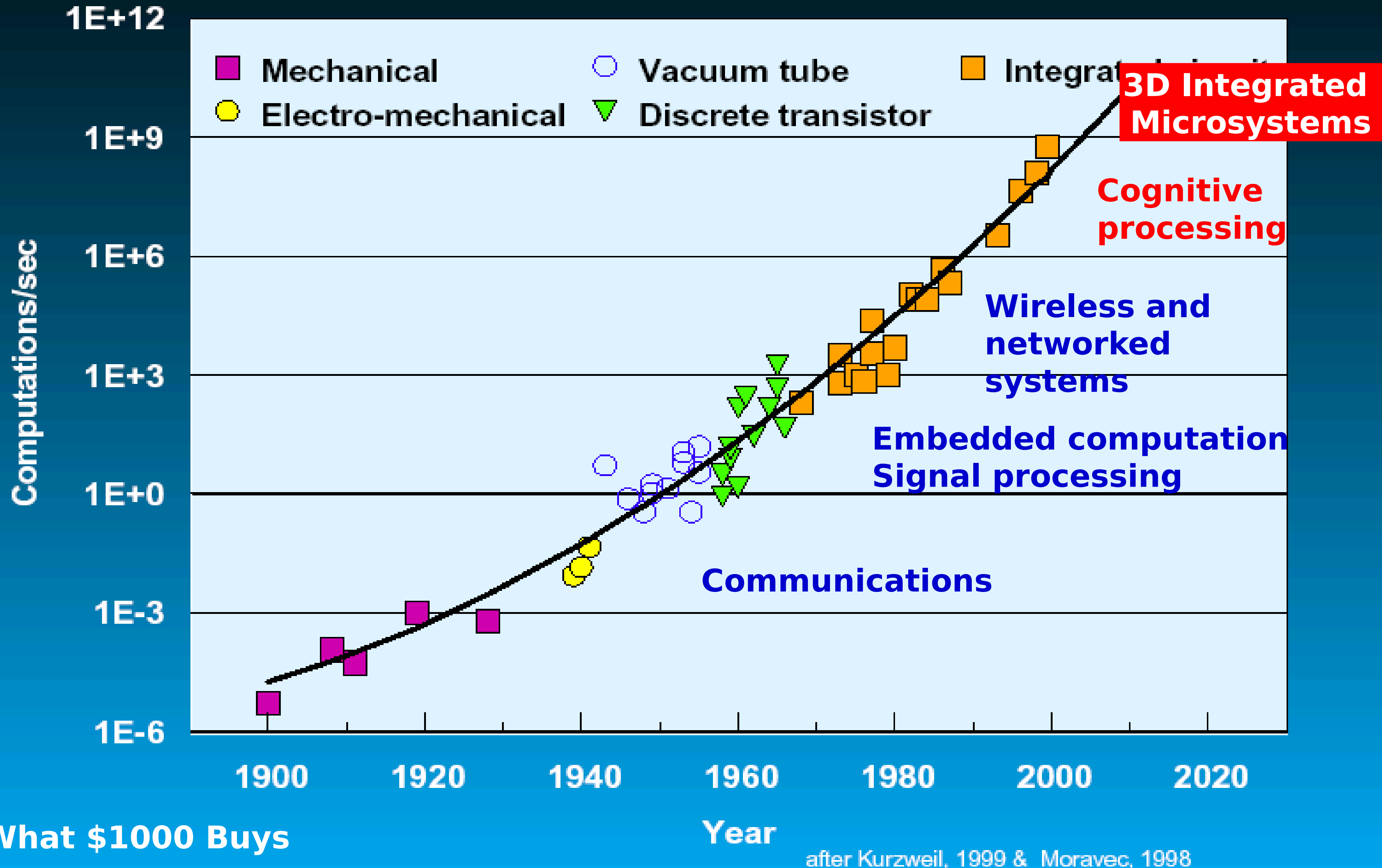
on the Technology Roadmap



Integrated Microsystem

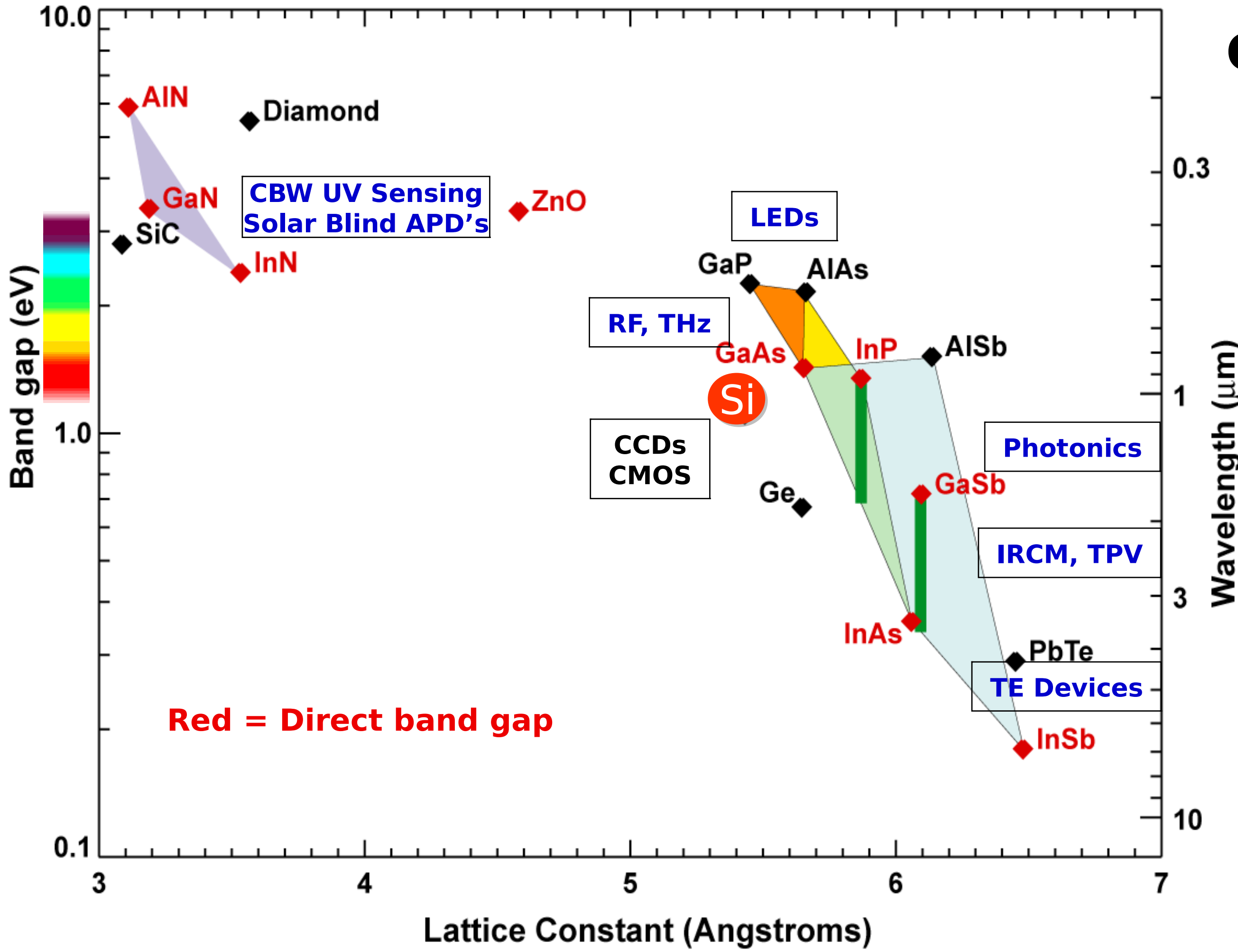


3D Integrated Microsystem



What $1000 Buys

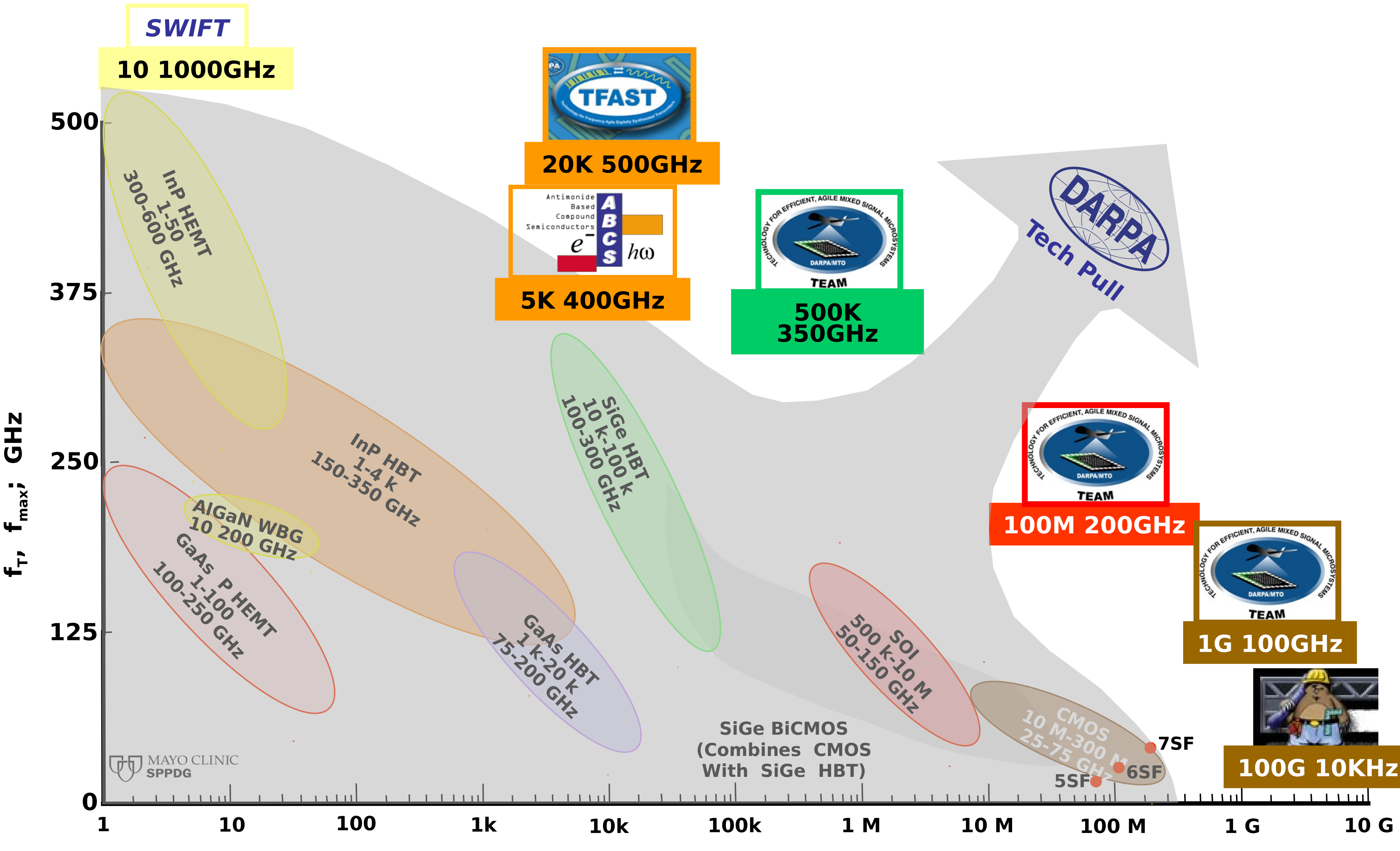
DoD's Need for Advanced Materials



Critical Applications

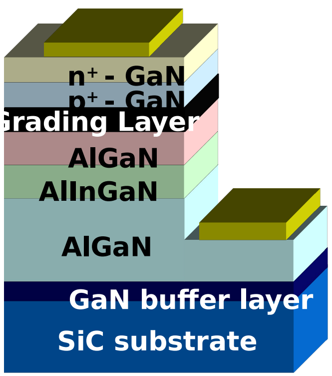
- IR detectors
- Thermophotovoltaic devices
- Solar blind UV detectors
- Lasers / LEDs
- Thermoelectric devices
- Optical waveguides and photonics
- THz Sources
- Microwave/mm-wave
- Power conversion

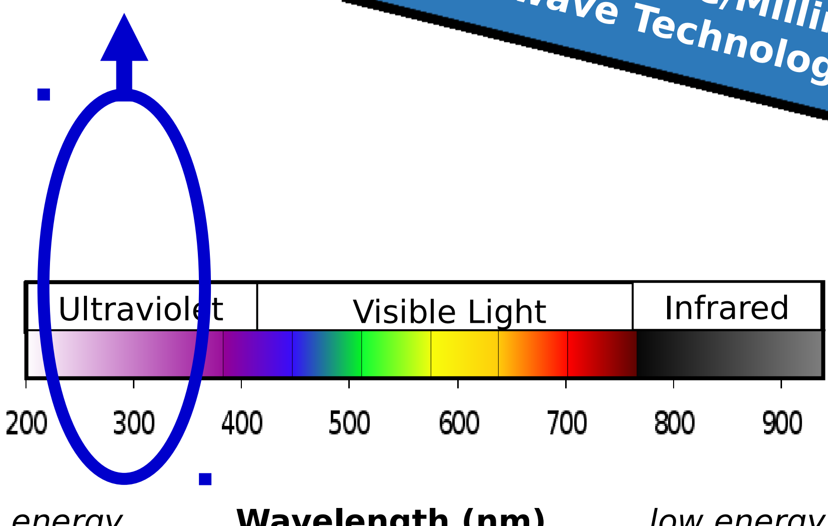
Integrated Ft Device Scaling



with
Wide Bandgap Materials

Materials Development

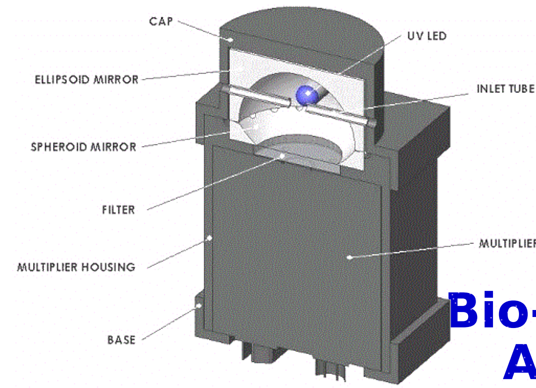




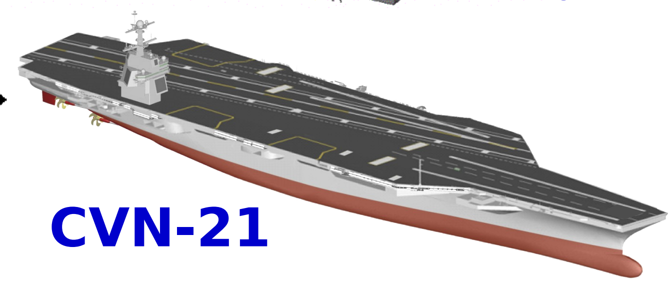
Semiconductor UV Optical Sources (SUVOS)

High Power Electronics (HPE)

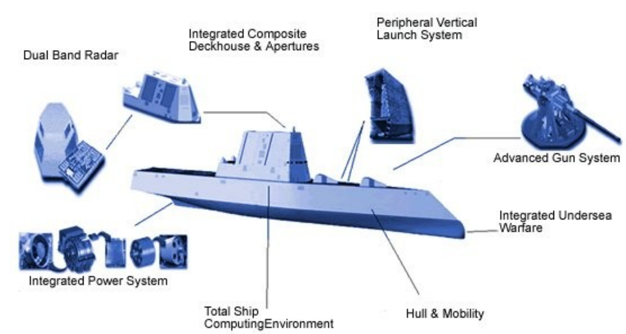
RF/Microwave/Millimeter-wave Technology



Bio-Threat Alarm



CVN-21



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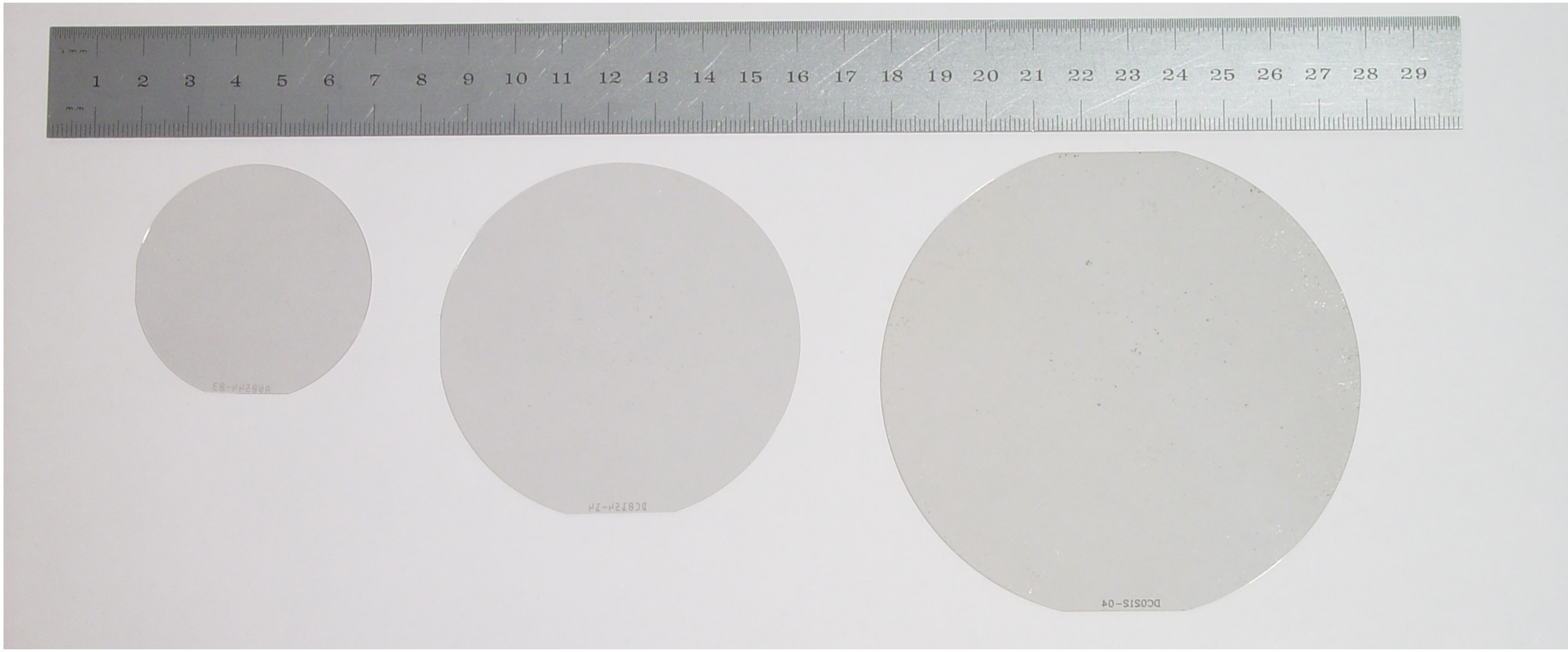
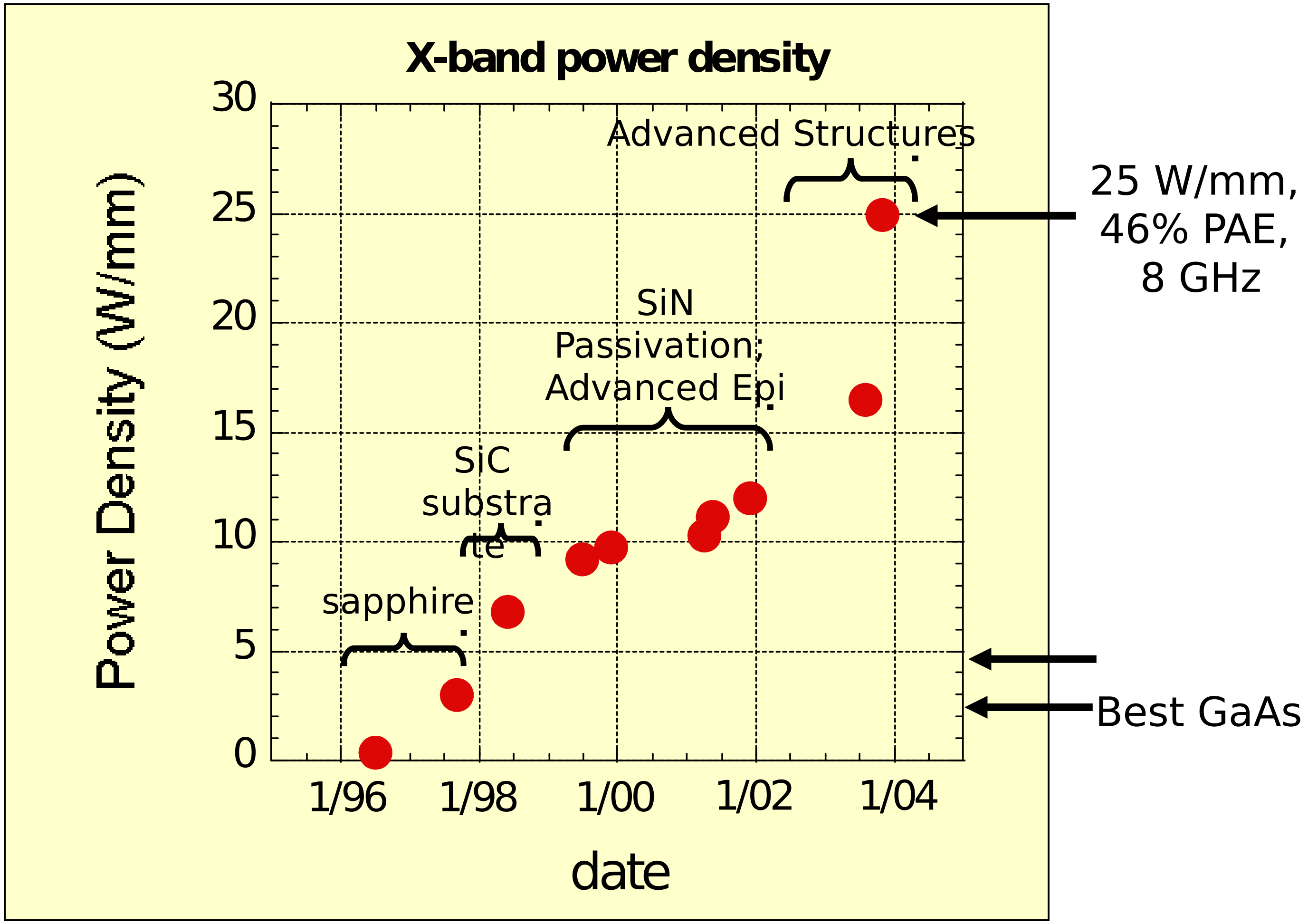
insulating SiC substrate size and quality



First demonstration of 100 mm diameter semi-insulating SiC wafers

Future focus: demonstrate WBG components with record power, efficiency, and linearity for DoD systems

Progression in GaN HEMT Power Density

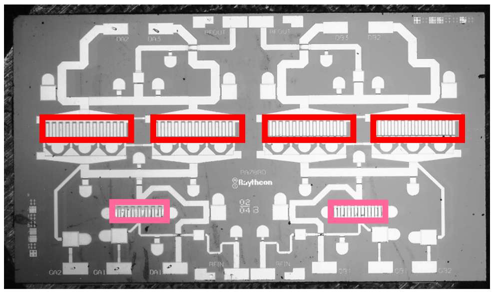


High Performance Amplifiers

10 W X-band GaN HEMT Device

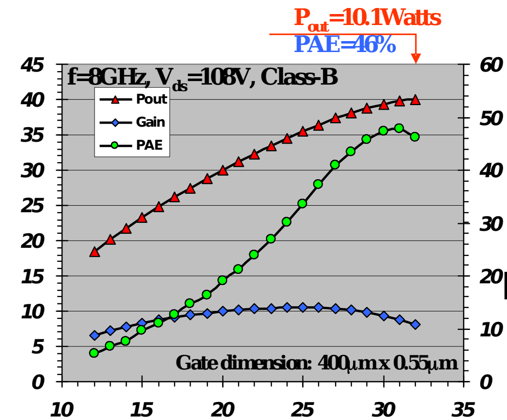
10 W X-band GaAs PHEMT amp

5.7mm x 3.3 mm



7V @ 75 mA/mm
PAE = 40%
~ 20mm total output gate periphery
R_{out} ~ 4.6Ω

Same power at 1/20 the footprint



FET:
0.4 mm periphery
Vds = 108 V,
Id = 425 mA/mm
PAE= 46%
R_{out} = 600 Ω

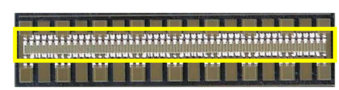
High impedance enables high efficiency and wide bandwidth

~10x the power in same transistor size

Commercial impact expected from superior linearity and efficiency

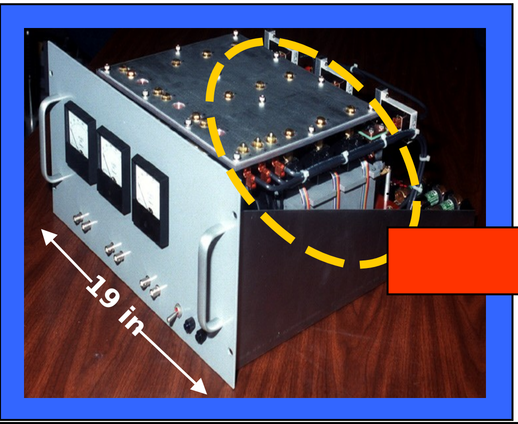
50 W (pulsed) X-band GaN HEMT Device

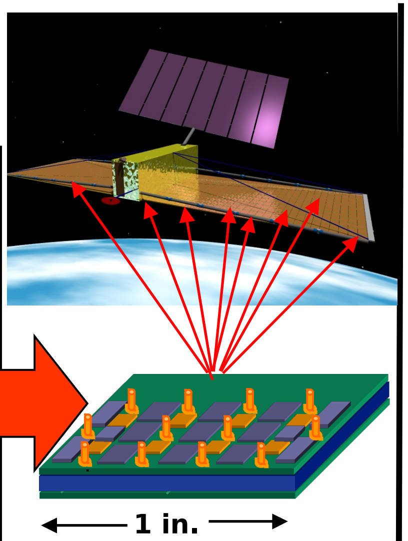
0.7mm x 4mm
(~1/2 GaAs output stage)



50V@ 250 mA/mm
PAE = 28%
12mm periphery
R_{out} ~ 15Ω

Robust Integrated Power Electronics (RIPE)





DESCRIPTION / OBJECTIVES / METHODS

- Develop new power semiconductors for highly efficient integrated solid state power electronic circuits in the 1-100kW range and harsh environment circuits, coupled closely to loads.
- Demonstrate high frequency switching capabilities in the 100MHz range, and subsequent substantial reduction in the size of associated magnetic devices, the key to reducing overall size of the power subsystem, and increasing its efficiency.
- Demonstrate capabilities to make integrated circuits for high temperatures (>250 degrees Celsius)

MILITARY IMPACT / SPONSORSHIP

- Smaller, lighter, more capable power electronics will enable significant increases in overall system efficiency by enabling the power delivery system to be dynamically coupled to the other electronics, providing point-of-use power directly at the load.
- This program will establish a capability to obtain extremely efficient power integrated circuits in a semiconductor technology that also potentially provides very high temperature circuits for sensors in harsh environments.

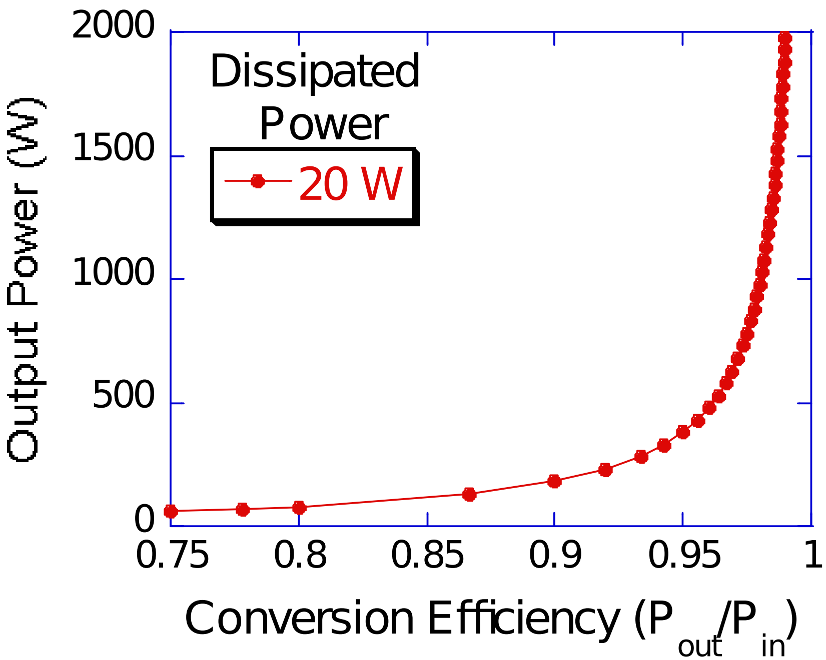
MAJOR PERFORMERS

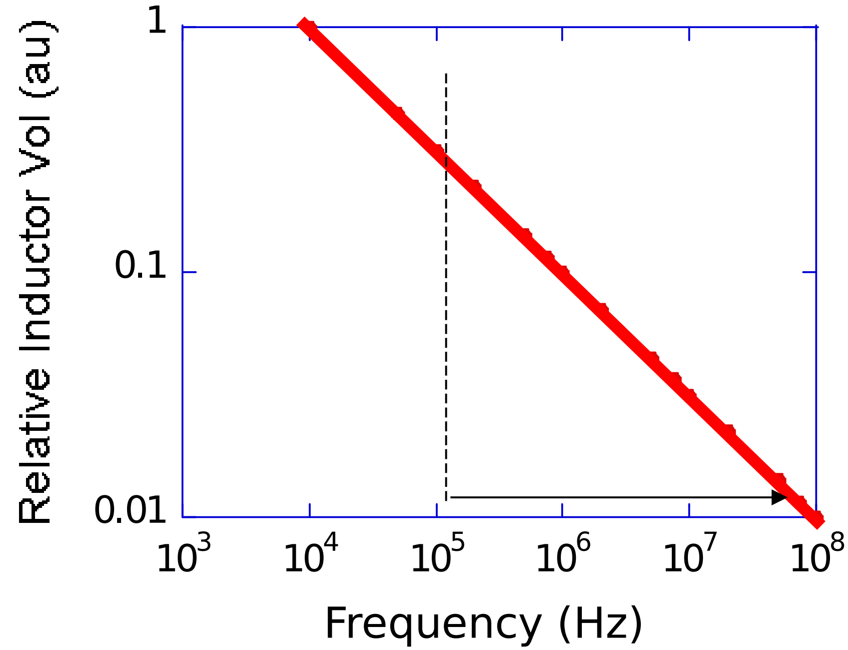
- To be determined
- Source selection sensitive

Miniaturization Enabled by Higher Efficiency and Frequency

$$P_{out} = \frac{efficiency \times P_{dis}}{1 - efficiency}$$

$$Inductor\ Vol \propto 1/\sqrt{freq}$$



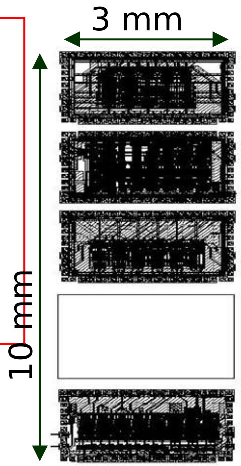


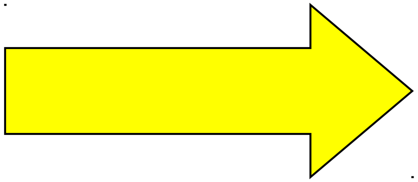
Increase available power to load with smaller volume

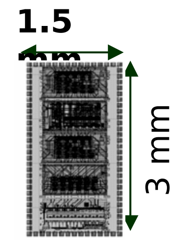
TFAST Objective

Super-scaled InP DHBTs in complex mixed signal circuits

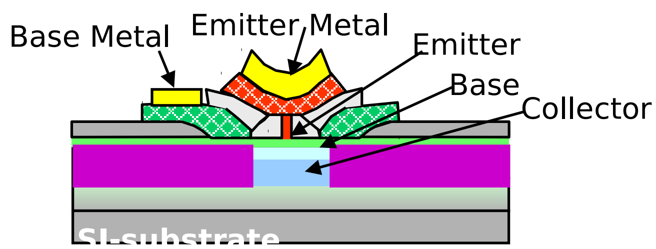
1 µm InP HBT DDS:
Power: 20W
Complexity: 4 chips @ 1200-2000 transistors ea
Max. Sample rate: 10 GHz
Size: > 30 mm²



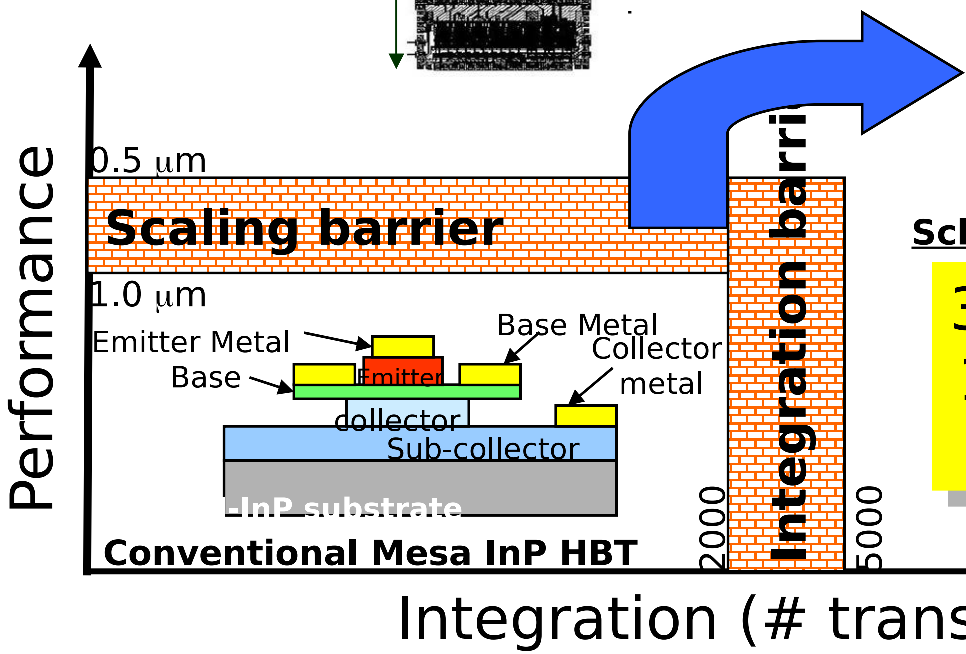




<0.25 µm InP HBT DDS: Power: 5W
Complexity: Up to 20,000 transistors
Max. Sample rate: 30 GHz
Size: 4.5 mm²

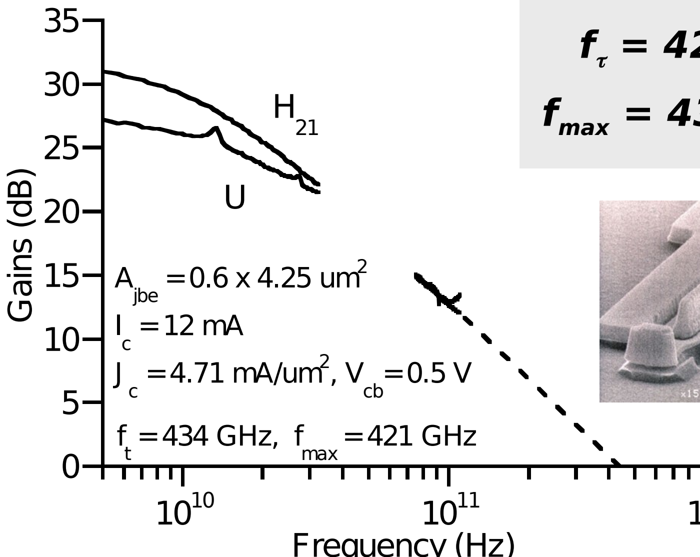


Schematic TFAST Scalable InP HBT



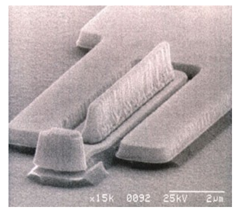
3x higher circuit speed
10x higher integration
10x lower power

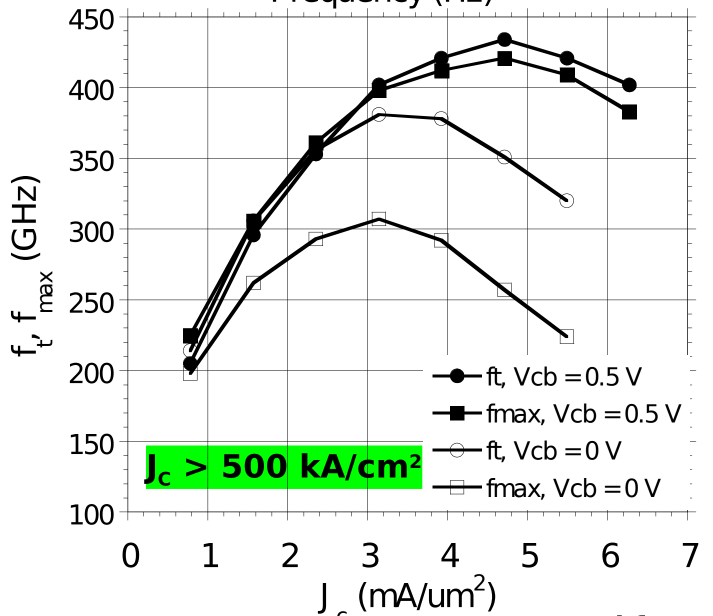
InP Double Heterojunction Bipolar Transistor with Record f_τ and f_{max}



f_τ = 420 GHz

f_{max} = 434 GHz



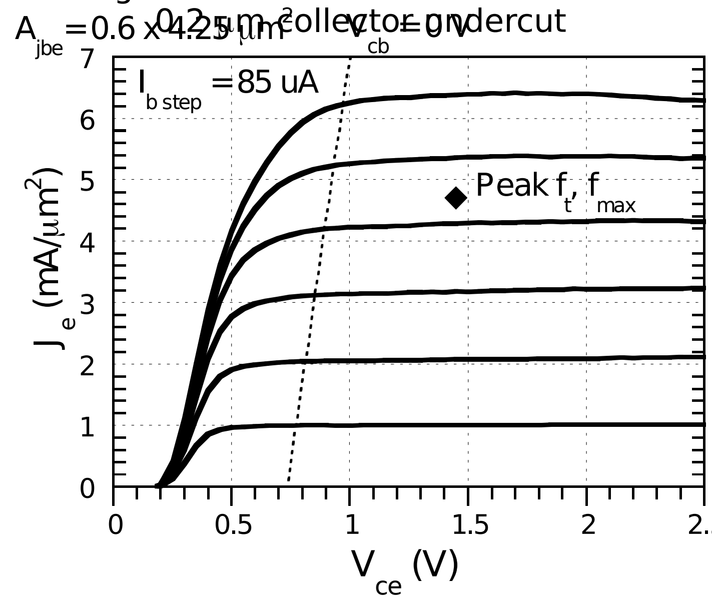


Critical Epi and Process Details

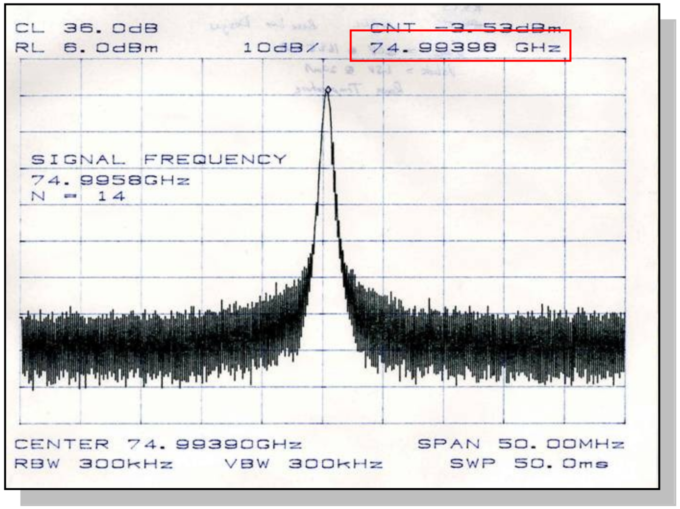
0.6 x 4.25 μm emitter
- 10 Ω-μm² contact resistivity

3 nm InGaAs base:
- $8*10^{19}/cm^3 \rightarrow 5*10^{19}/cm^3$
- 564 Ω/square
- 0.3 μm wide base contacts
- 25 Ω-μm² contact resistivity

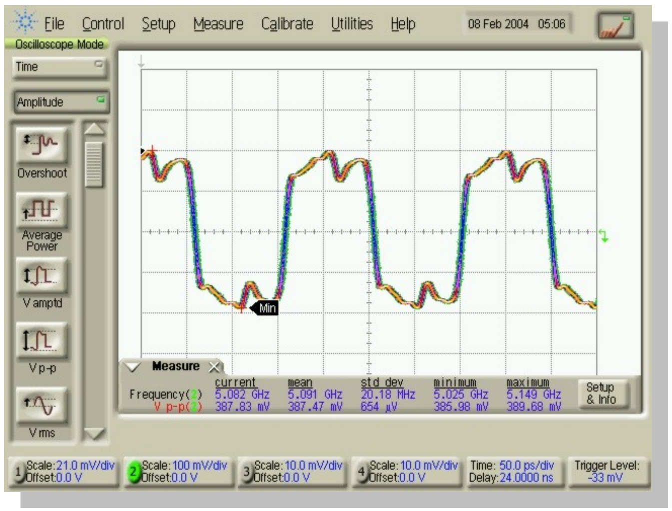
15 nm InP collector
- 20 nm InGaAs setback layer
- 24 nm InGaAlAs superlattice grade
- 0.2 μm collector undercut



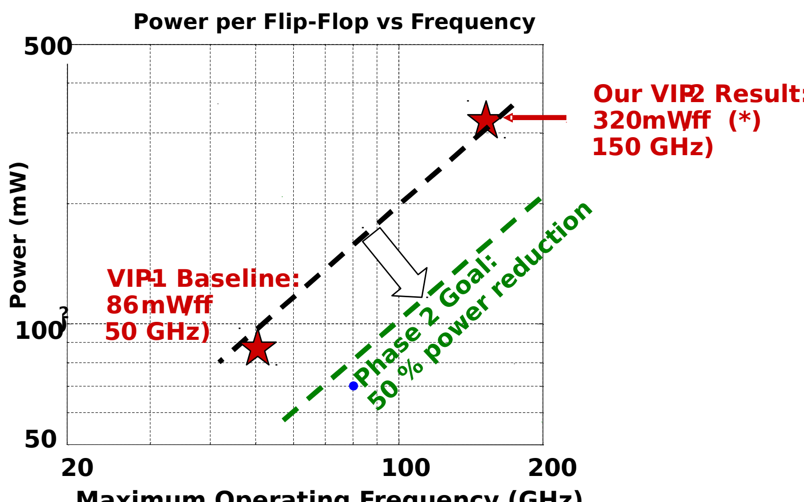
150 GHz maximum operating speed



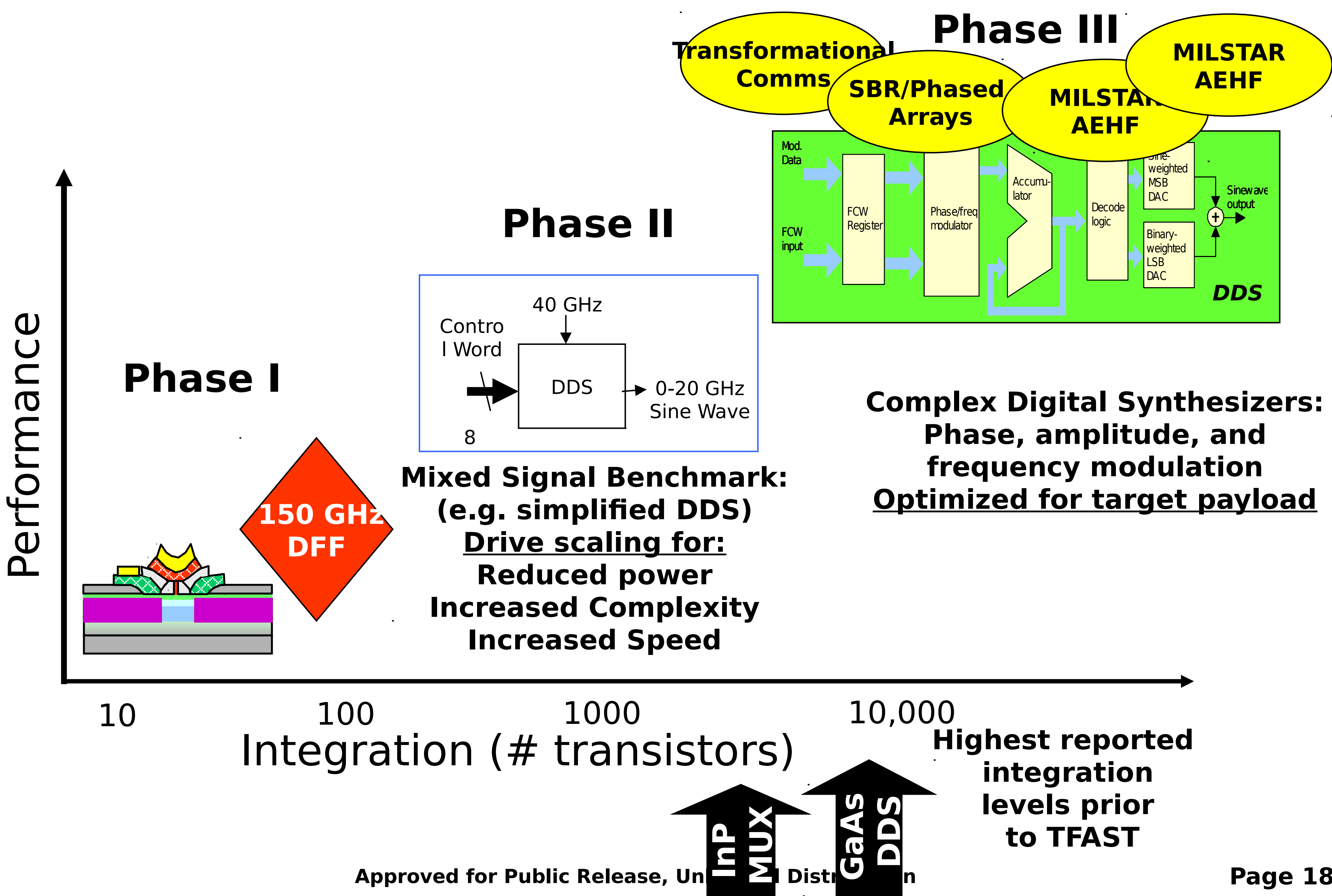
Static operation confirmed at 10 GHz



All test results have been confirmed by Mayo Foundation

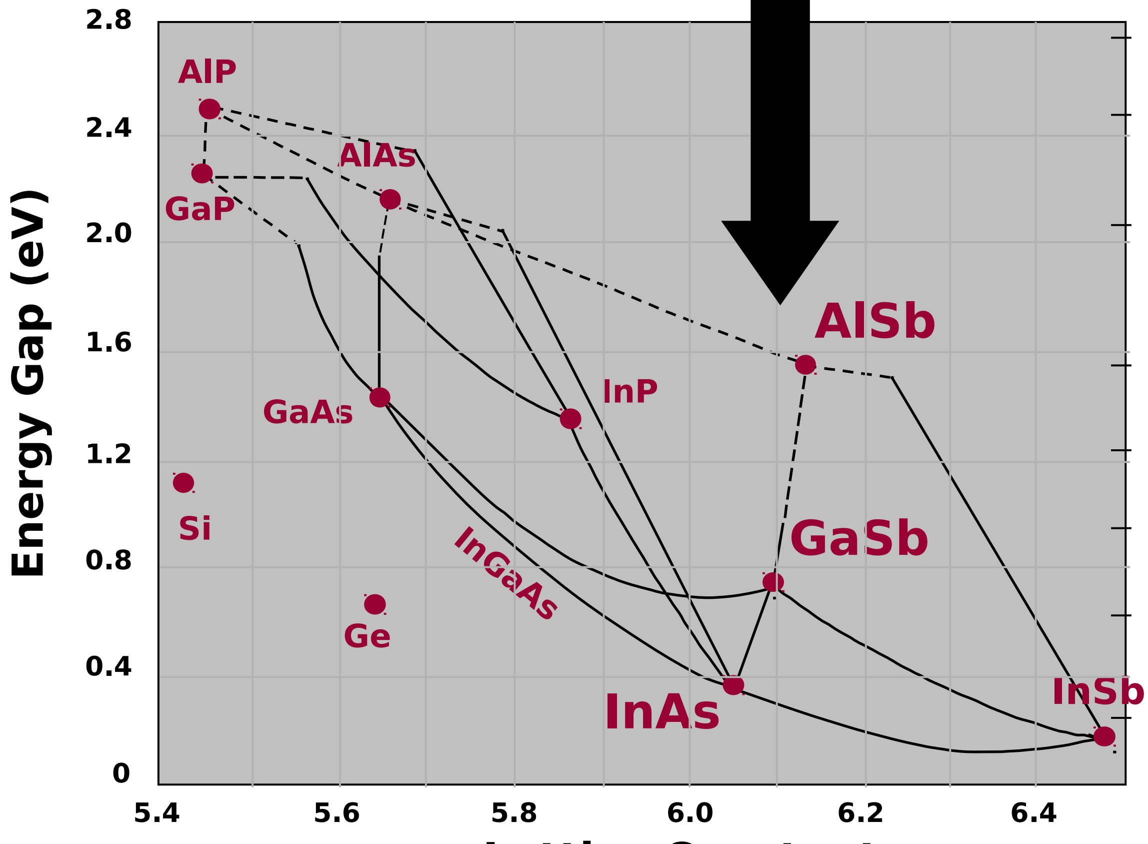


Phase II/III Strategy

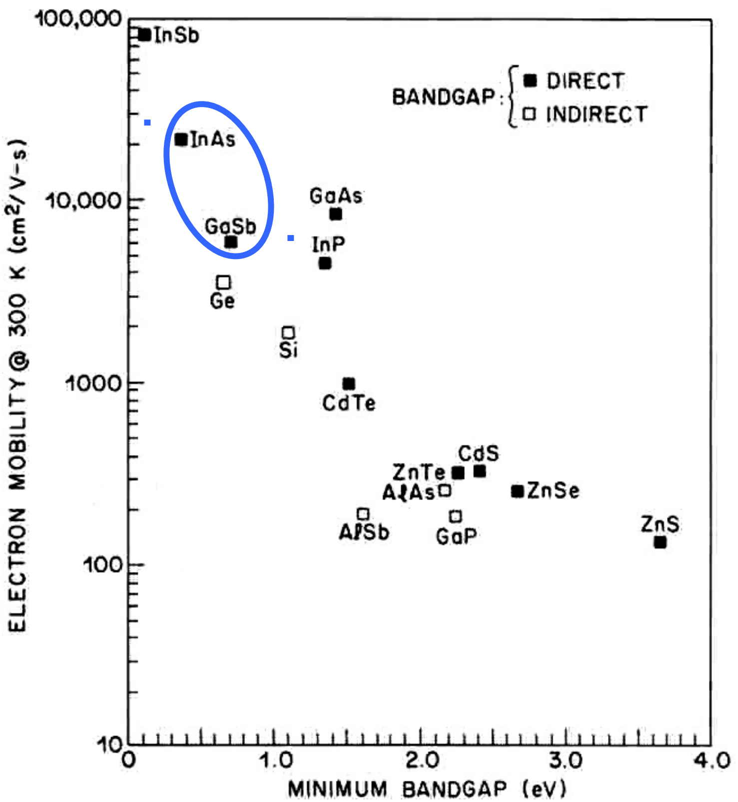


ABCS Material System

6.1 Å III-V Materials

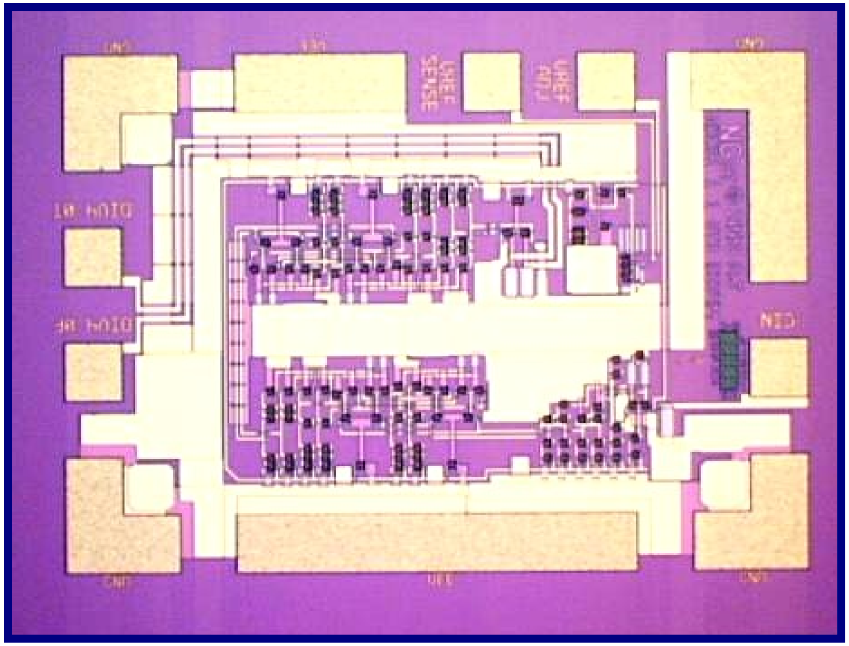


Electron Mobility



The main focus of the ABCS program is to demonstrate integrated circuits with ultrafast speed and low consumed power

ABCS LNA Circuit Development



F_{clock} = 21.2 GHz

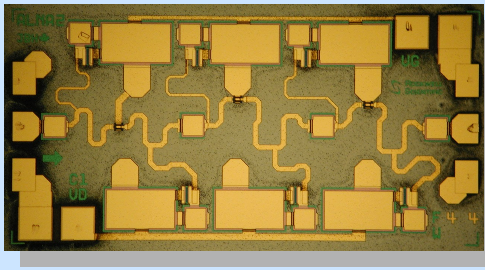
F_{output} = 5.3 GHz

High InAs / AlSb MMIC Integration

Demonstrated a divide by 4 circuit with ~ 100 HBTs
operating at fclock = 21.2 GHz

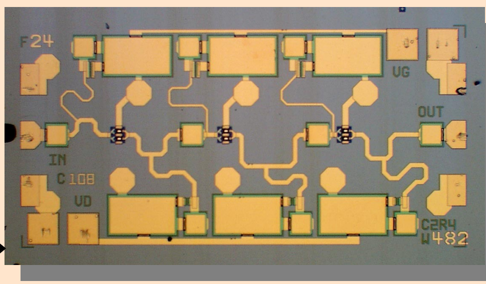
ABCS

Ka-Band LNA
0.35V, 12mA Fets
Gain = 28dB
NF < 2.2 dB
Power = 4.2mW



GaAs

Ka-Band LNA
4V, 40mA Fets
Gain = 20 - 27dB
Power = 160 mW



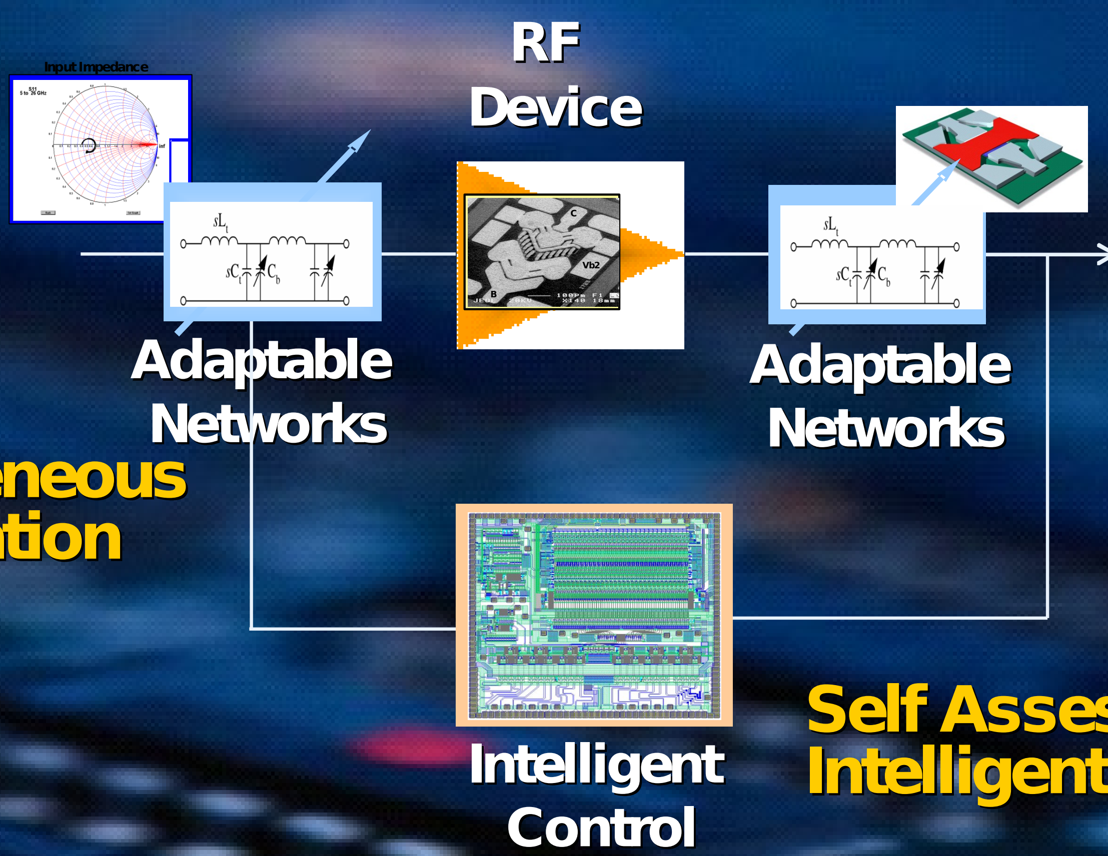
Part currently used in PAC-3

World's First InAs / AlSb MMICs

3-Stage Ka-Band LNA Using only 4.2 mW DC Power
~40 X Less Power than GaAs with Equivalent Performance

Intelligent RF Front Ends

Real Time Adaptation



Heterogeneous Integration

Self Assessment and Intelligent Control

Enabling Adaptive Multifunctional RF Sensors for Rapid Changing Environments

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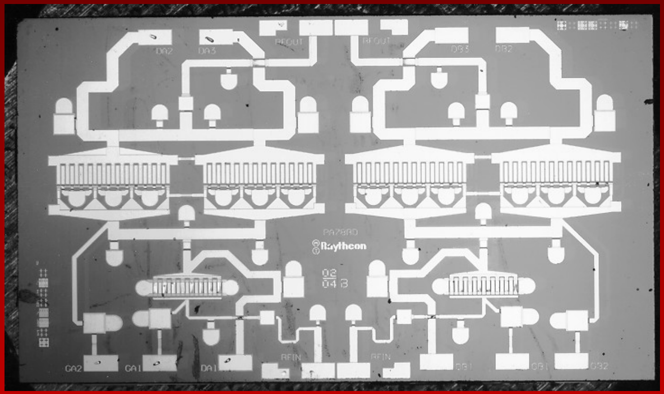
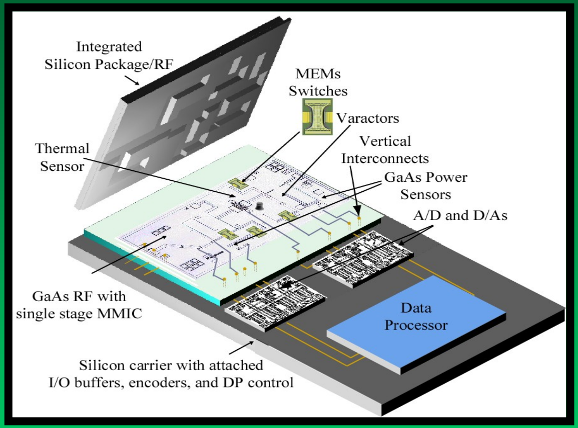
Beyond MMIC's



MMIC Amplifier

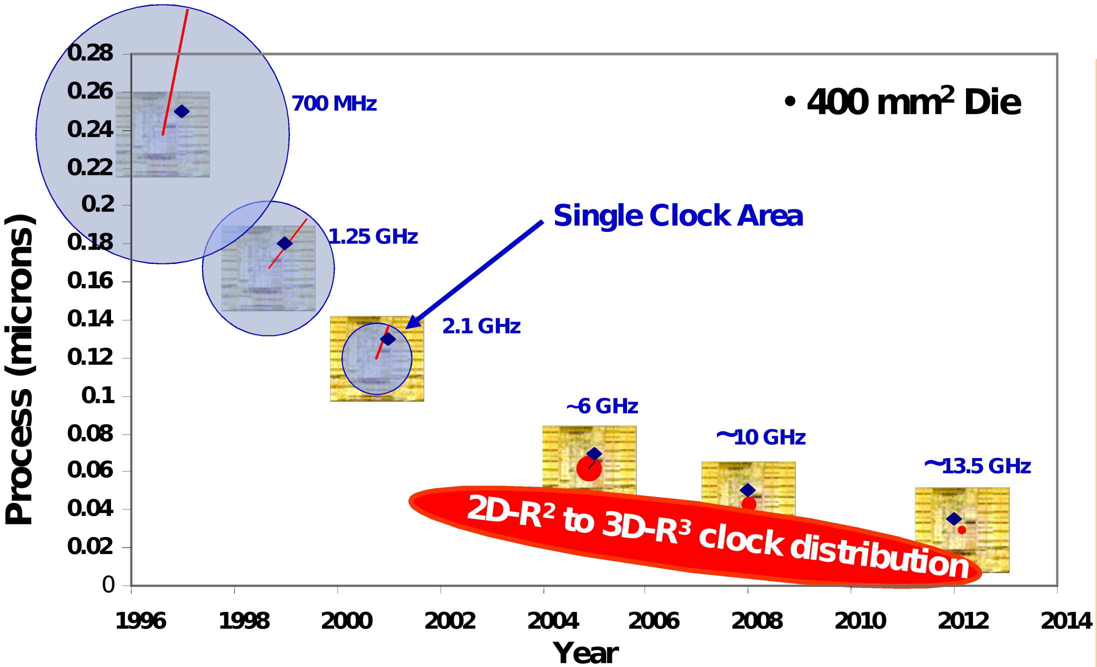
- Optimized for a given function
- Rely on consistent fabrication processes and device models
- Bandwidth-performance trade-off

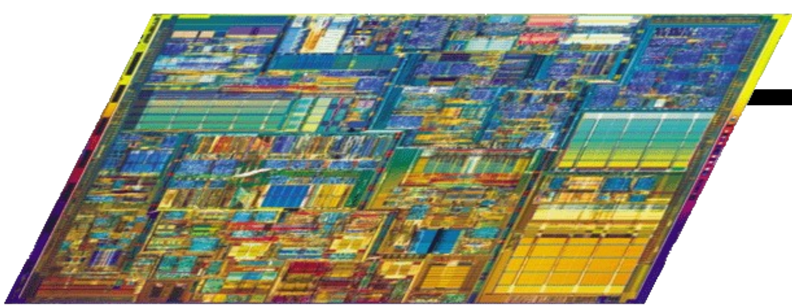


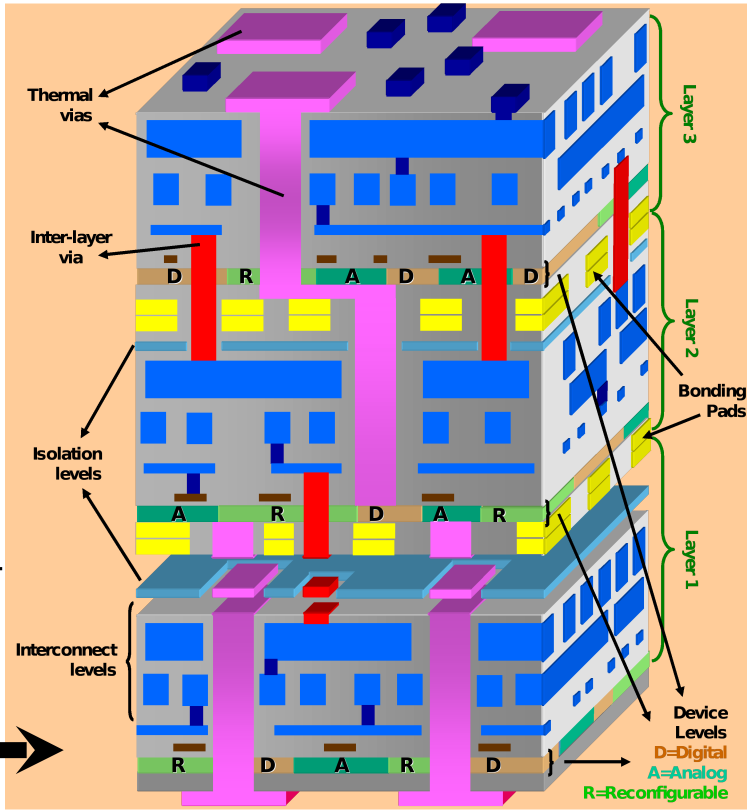
IRFFE Amplifier

- Adaptable/Tunable
- Continue self assessment and self optimization
- Tolerant of device and fabrication process variations

3D Integrated Microsystems





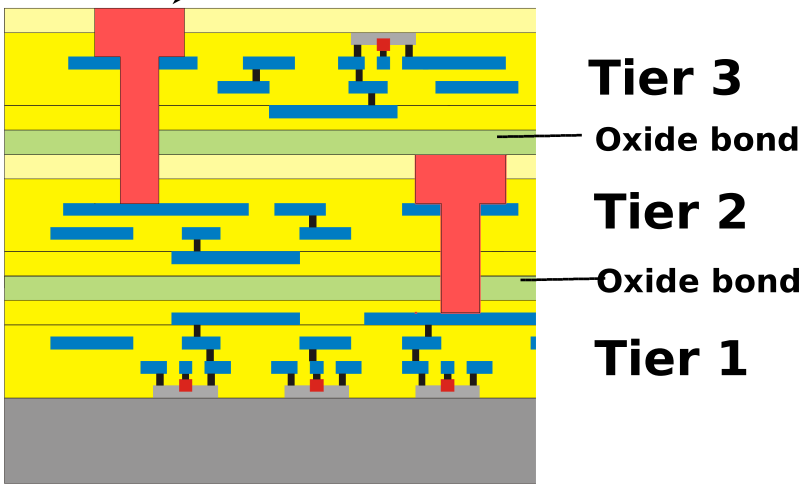


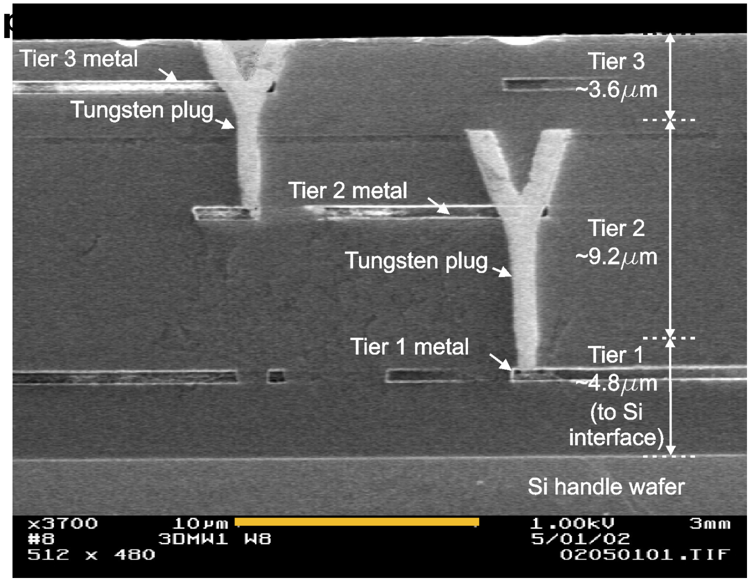
Semiconductor Industry 2D Scaling

3D Integrated Microsystem

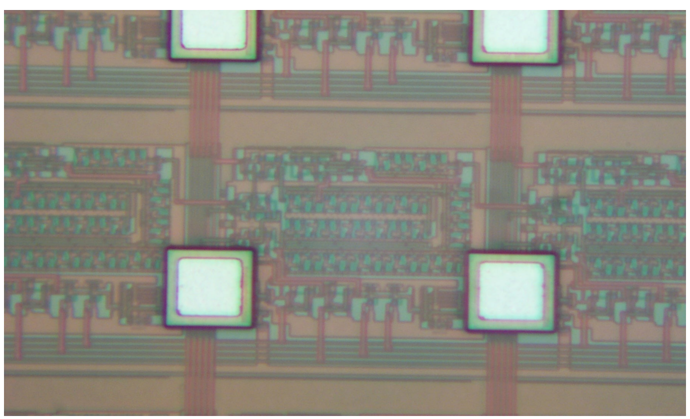
3D Integration of SOI Circuit Layers

Sub-micron interlayer connections (tungsten p



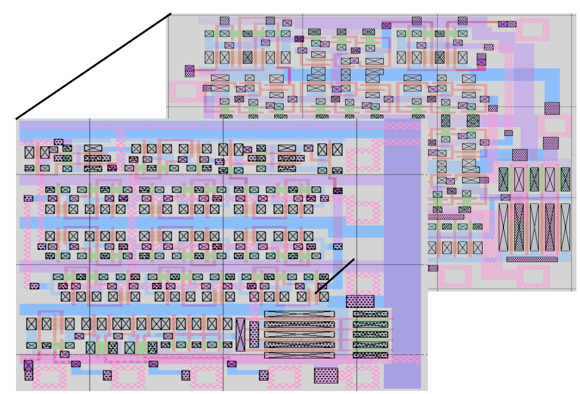


CMOS 2001 Ladar Chip



One tier of bulk CMOS 100-µm pixel ~1-ns timing

VISA Ladar Chip



Multiple tiers of FDSOI CMOS 30-µm pixel ~100-ps timing

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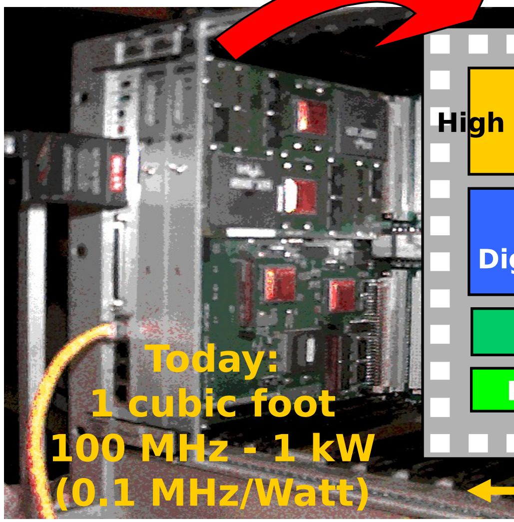
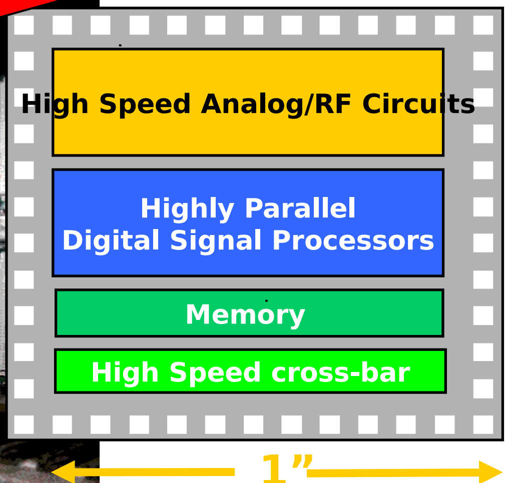
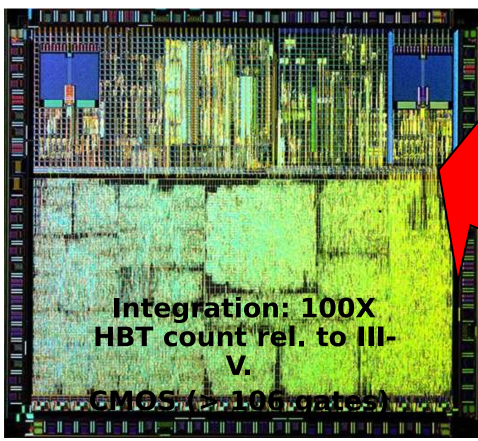
Technology for Efficient, Agile Mixed Signal Microsystems (TEAM)







TEAM :
1 square inch
Mixed Signal
System-on-Chip

10’s GHz, 10’s W

Goal:

Demonstrate silicon (SiGe) devices with f_t > 200GHz in low power circuits operating at up to 60GHz that deliver III-V device performance @ integration levels of 10K analog/RF devices & with submicron CMOS capable of > 10M transistors/chip to provide advanced, single chip RF systems

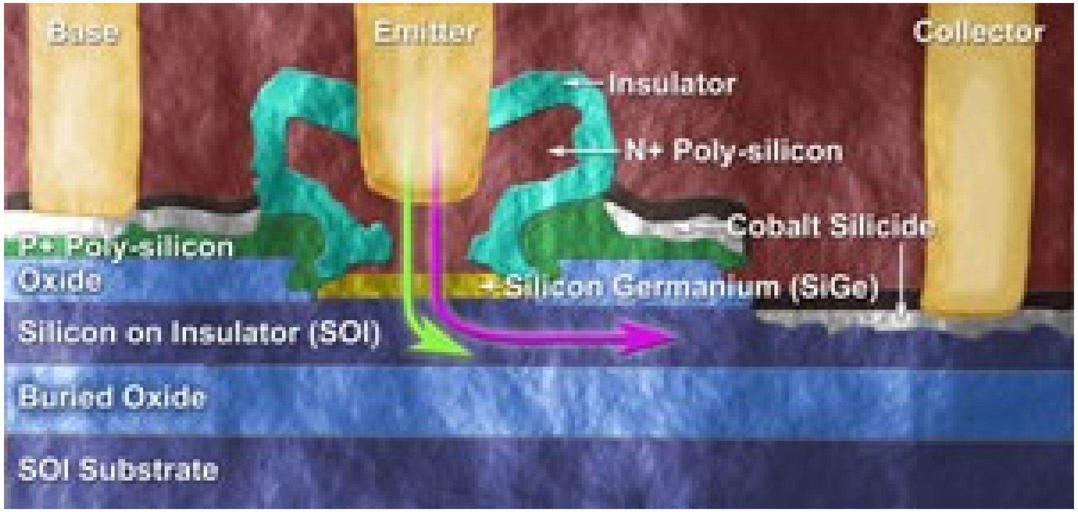
Challenges:

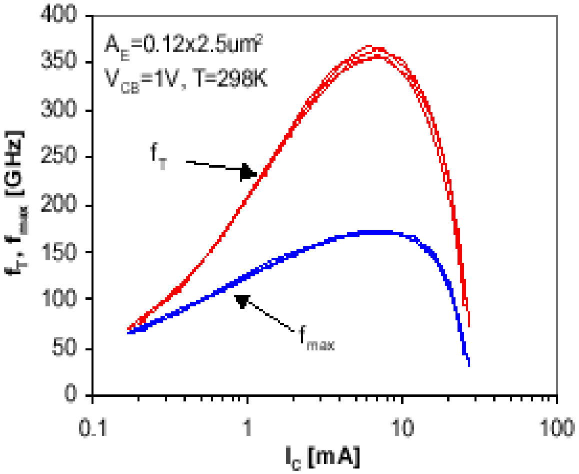
- **High f_T, high gain silicon devices with low output conductance, low noise figure (<2dB @ 20GHz), high linearity and low power dissipation**
- **Techniques to achieve isolation between RF and digital blocks (~ 100dB) and on-chip Qs of >20**
- **Device integration levels for complex, single chip RF systems**

Integrated chip-scale radar & radio transceivers with high performance, real time signal processing

Extending Si-based Transistors to >200 GHz Operation

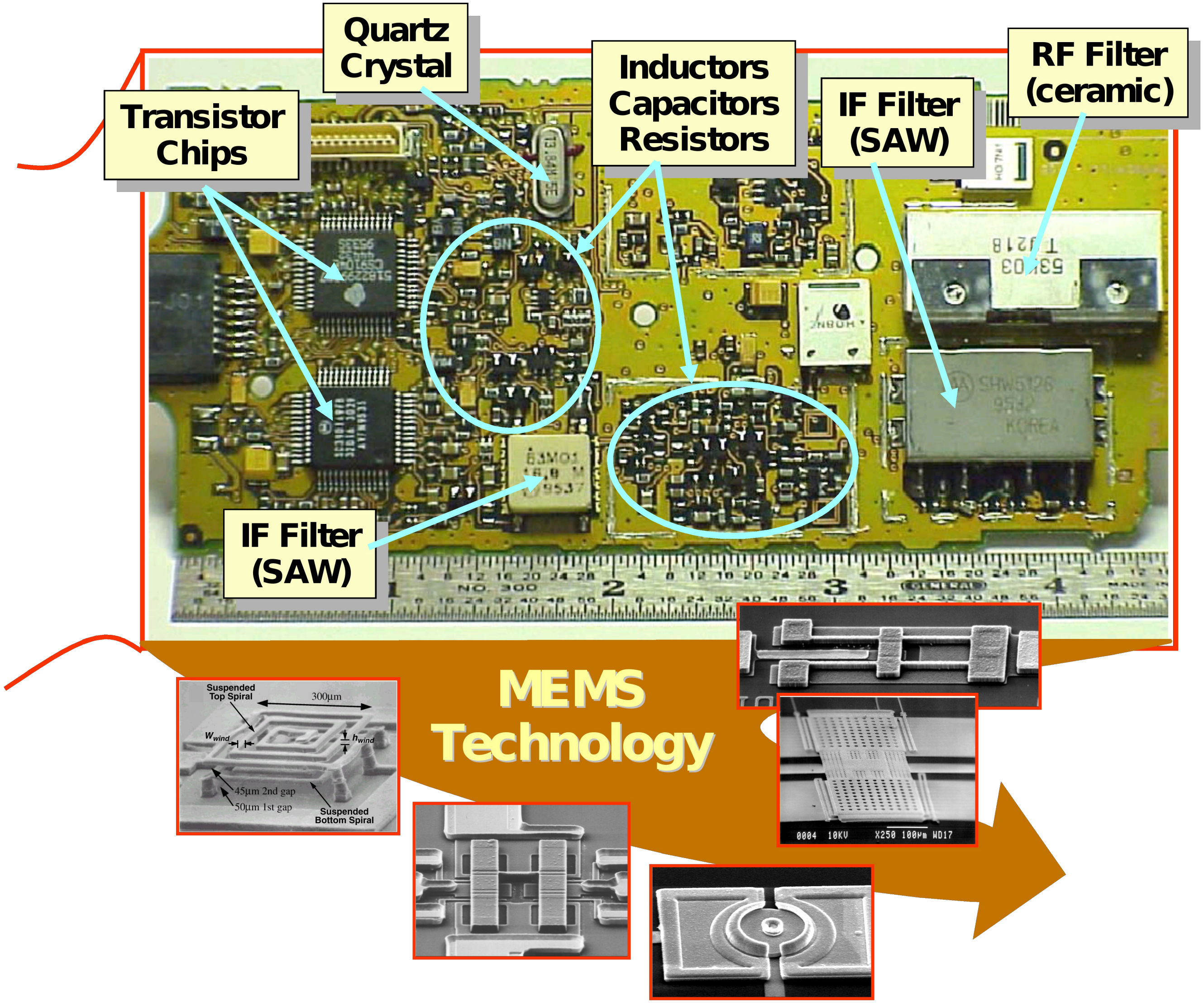
Cross-section of SiGe SHBT



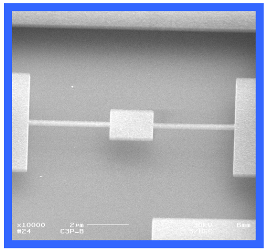


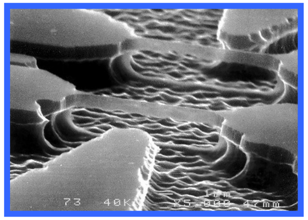
350 GHz IBM 0.12 μm SiGe SHB

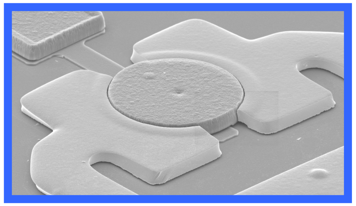
MEMS Provides Size Reduction

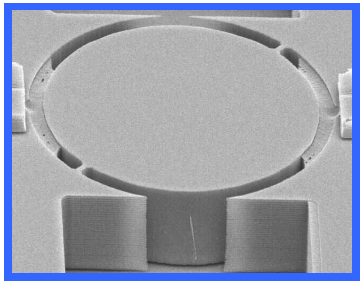


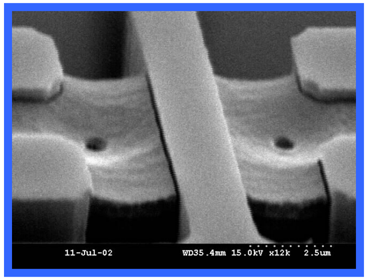
Nano-Mechanical Array Signal Processor (NMASP)



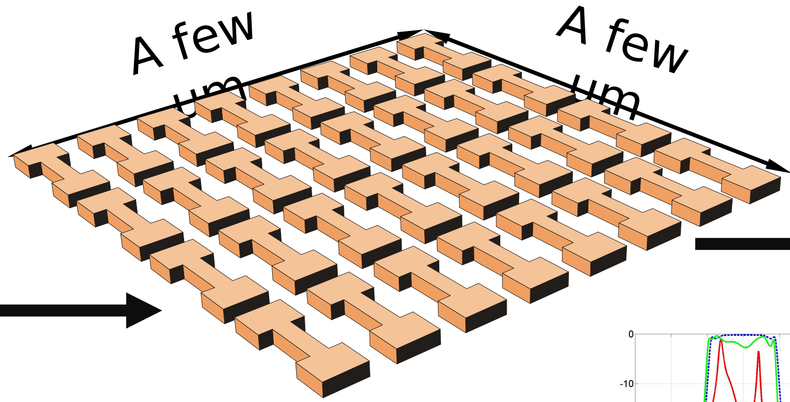


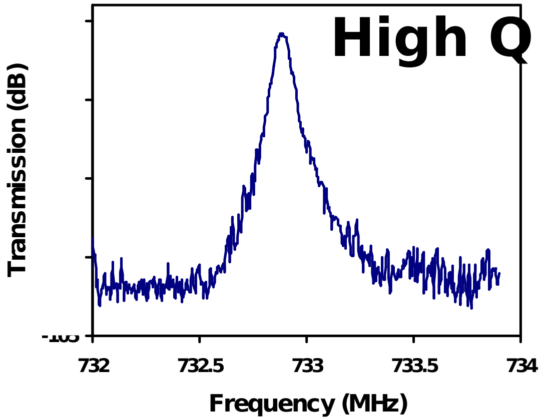




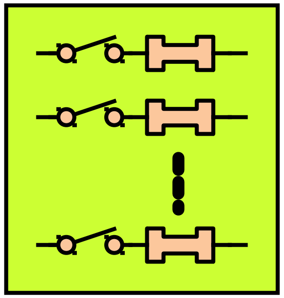


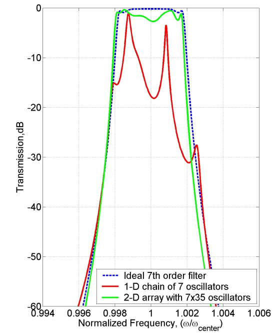
Materials and Resonator





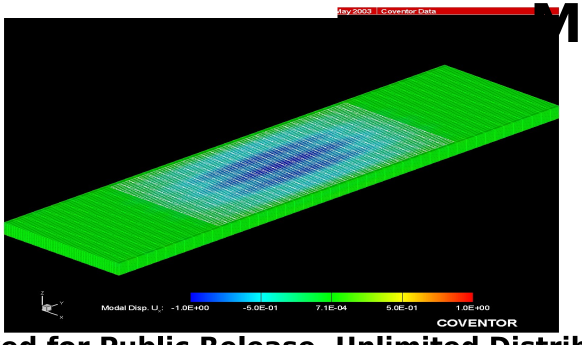
High Q

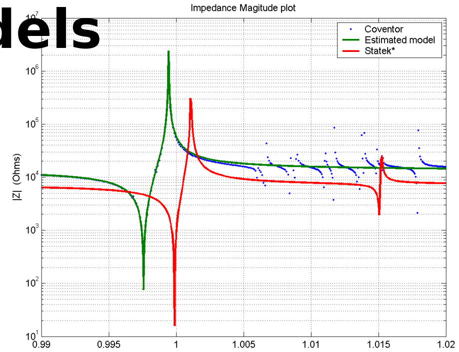




Filters

Verified Design Models





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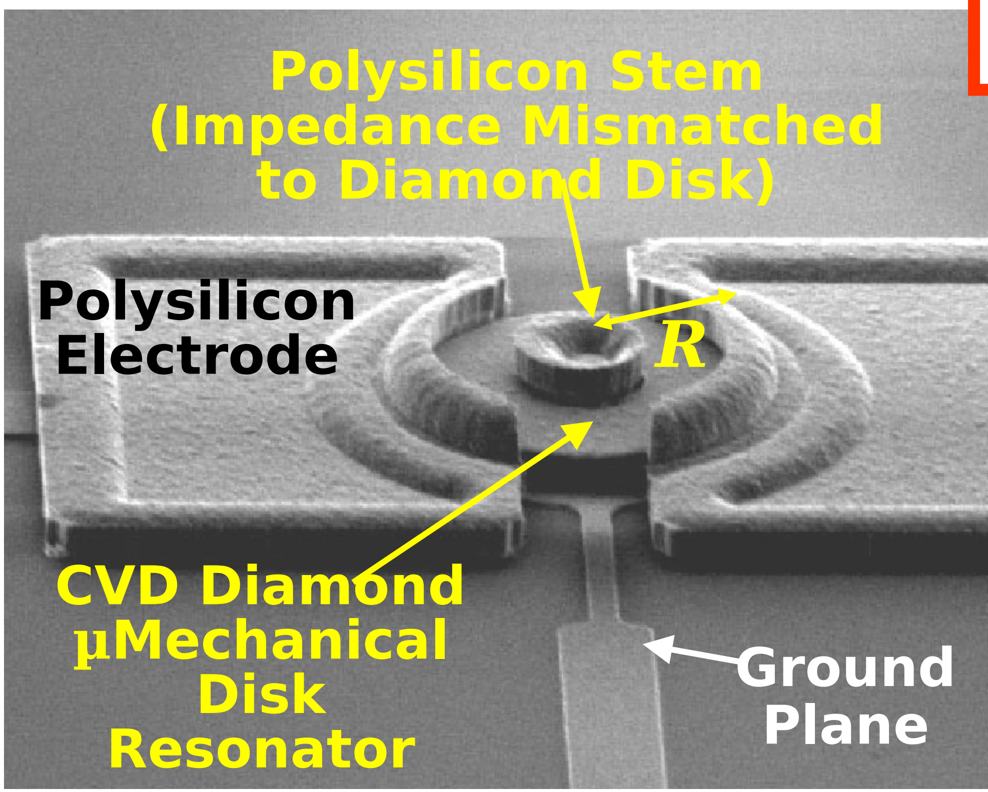
1.51-GHz, Q=11,555 Nanacrystalline Diamond Disk μMechanical Resonator

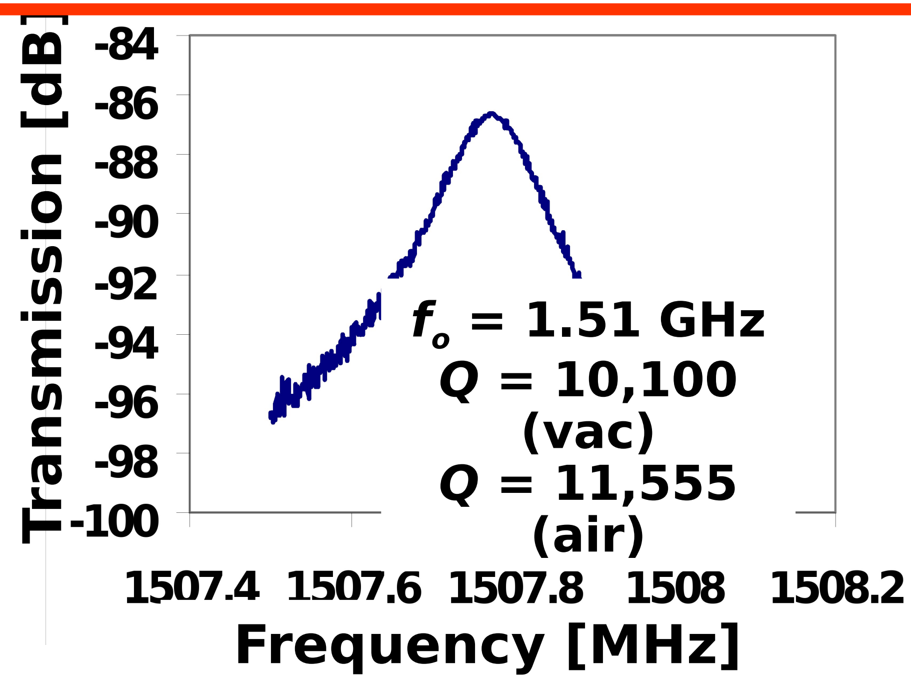
- Impedance-mismatched stem for reduced anchor dissipation
- Operated in the 2nd radial-contour mode
- *Q* ~ 11,555 in vacuum; *Q* ~ 10,100 seen even in air
- *Below*: 20 μm diameter disk

Design/Performance:

R=10μm, t=2.2μm, d=800Å, V_P=7V

f_o=1.51 GHz (2nd mode), Q=11,555

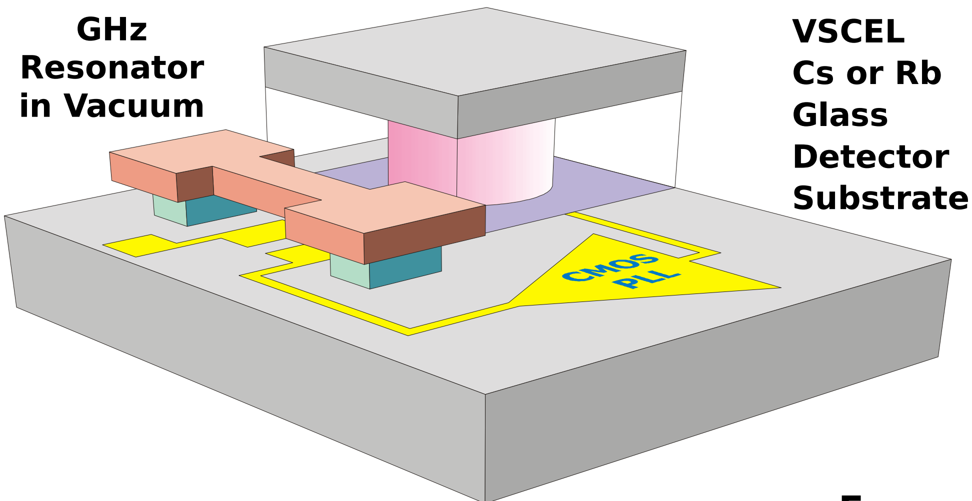




[Wang, Nguyen 2003]

3D Chip Scale Atomic Clock

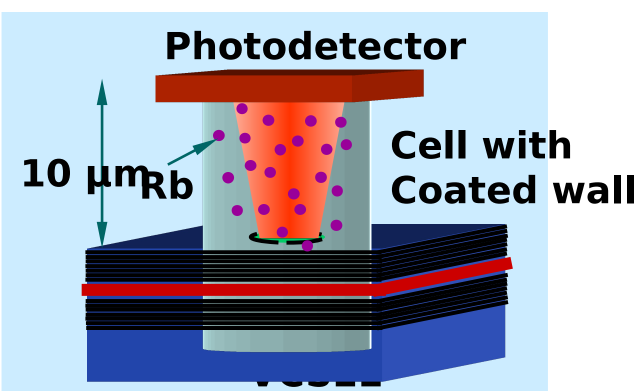
Ultra-miniaturized, low-power, atomic time and frequency reference units



>200X reduction in size

>300X reduction in power

($\pm 1 \times 10^{-11}$ accuracy $\Rightarrow$ <1µs/day)

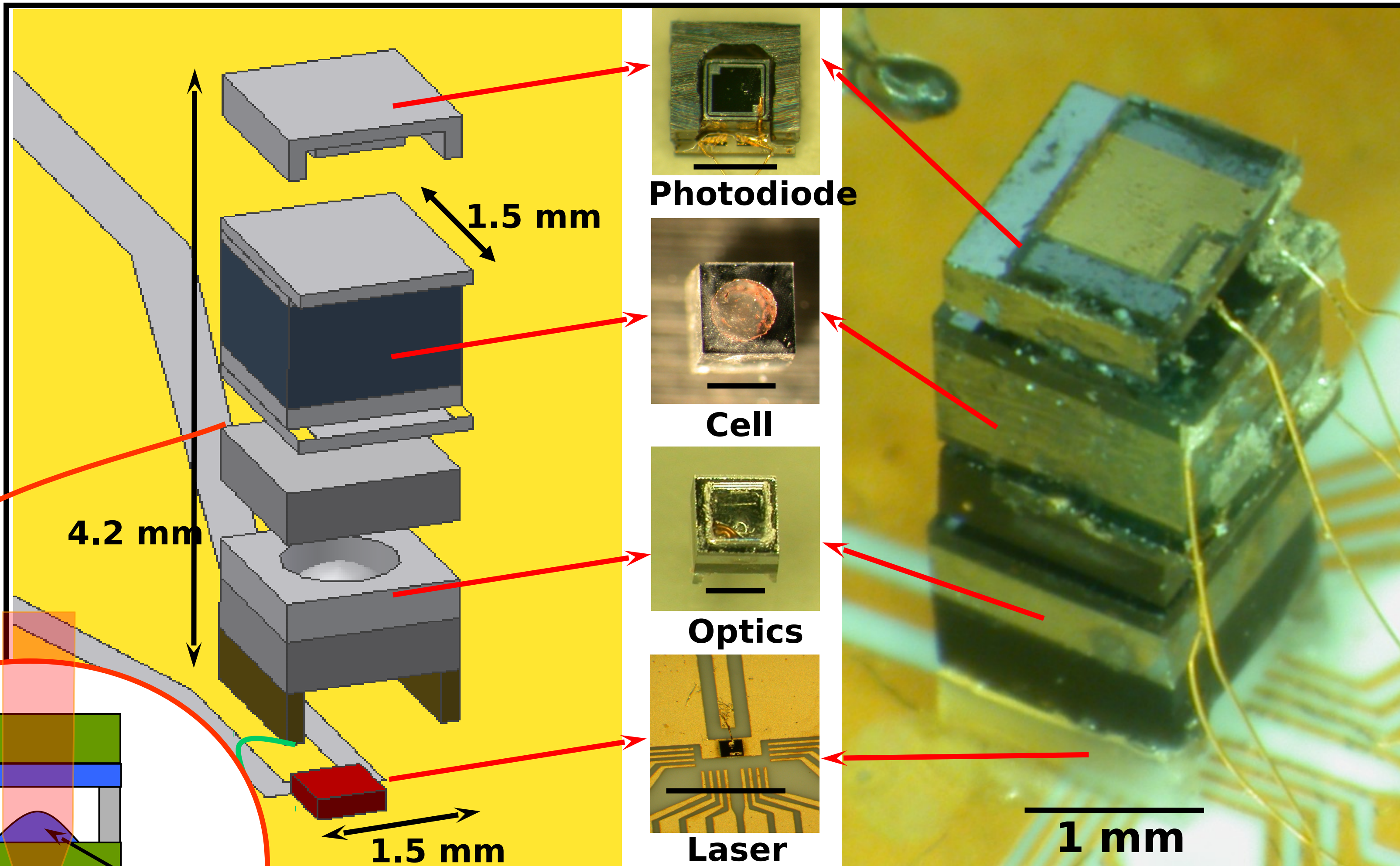


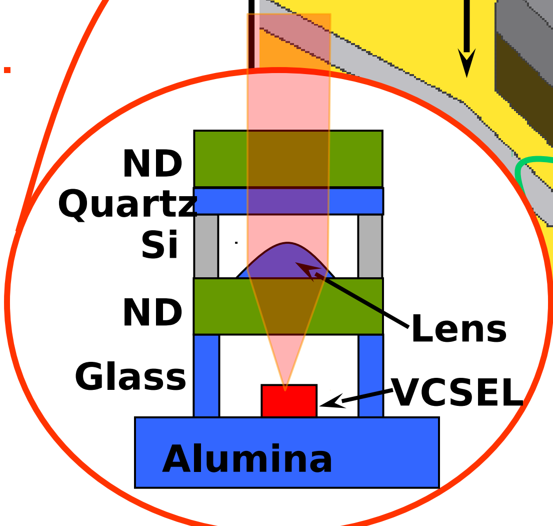
Atomic Absorption Cell

Example of Use: Radio System (SINCGARS)

Clock accuracy of $1 \times 10^{-11} \Rightarrow$ 16-hour resynch interval or radio silence

First Chip-Scale Atomic Physics Package

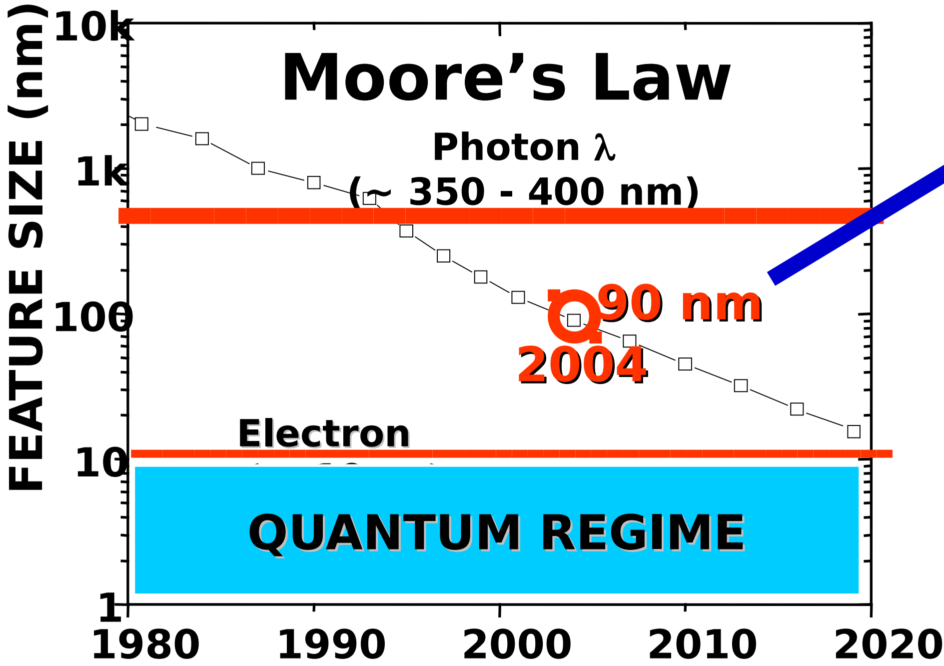




Total Volume: 9.5 mm^3 Stability: 2.4 x 10^{-10} @ 1s

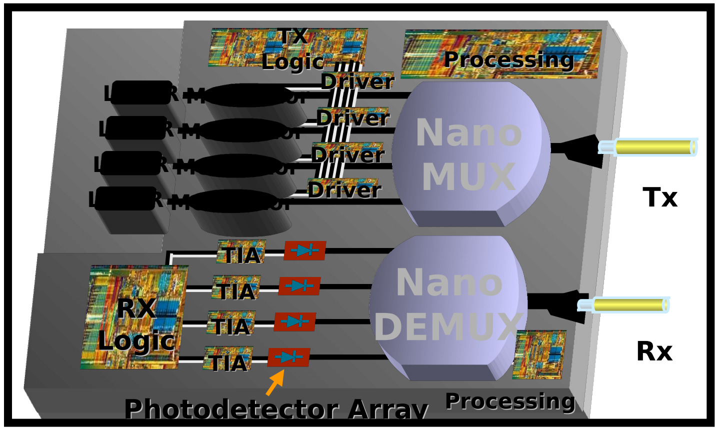
Cell Interior Vol: 0.6 mm^3 Power Cons: 75

Electronic/Photonic Integrated Circuits (EPIC)



Silicon Nanophotonics

- Small index contrast makes current devices very large
- Large index contrast in
- Si/SiO_2 + 90 nm fab capabilities (e.g. smooth walls) nanophotonics
- Fine Feature Size
  - **Essential** for very high speed



Silicon Nanophotonics
+
CMOS Electronics
Monolithically Integrated
VLSI Photonics and Electronics
on a single Silicon Chip
In a standard
CMOS-SOI Foundry

EPIC Challenges

Demonstrate a complete suite of nanoscale photonic and optoelectronic devices integrated with electronics to enable a "system on a chip"

MODULATOR
> 10 GHz
DRIVER

DETECTOR
> 10 GHz
QE
DARK CURRENT
NEP
TIA, CDR

MUX/DEMUX FILTERS
NANOSCALE
LOW LOSS
ADAPTIVE CONTROL, μP

EPIC CHIP

- Integration
- Device development
- Novel devices

PHOTON COUPLING
NANOSCALE
LOW LOSS

PASSIVE PHOTONICS
(WAVEGUIDES, SPLITTERS, TAPS…)
LOW LOSS

CONTROL

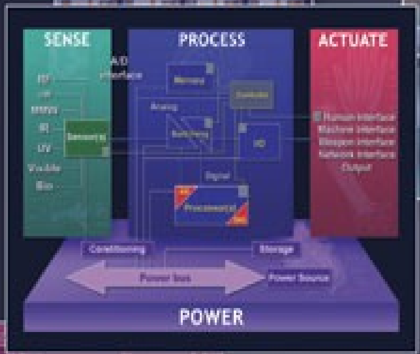
Fundamental Challenge
Silicon is an indirect bandgap material
(Long τ, no laser)

LASERS
AMPLIFIERS
λ CONVERTERS

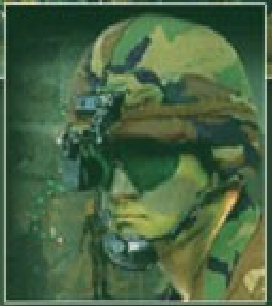
STATE-OF-THE-ART
CMOS/SOI
FOUNDRY

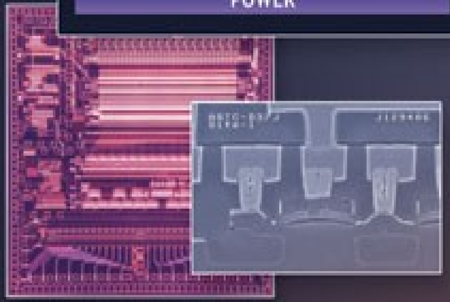
DIGITAL/ANALOG
DRIVERS/PREAMPS
INTERFERENCE

Scalable and affordable access to leading edge components



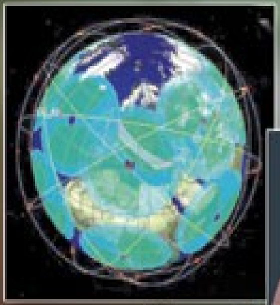
Microsystems for spectral exploitation and sensor dominance

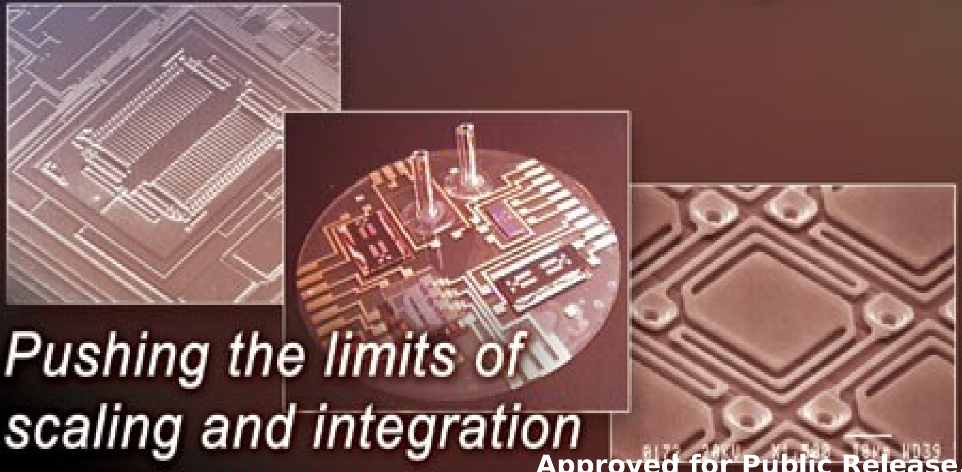




MICROSYSTEMS TECHNOLOGY OFFICE

DoD Access to Winning Microsystem Technology





Pushing the limits of scaling and integration

Systems that interact with the environment

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